Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S5 (S,FE) (FT/WP/S3PT) Examinations June 2026 (2019 Scheme)

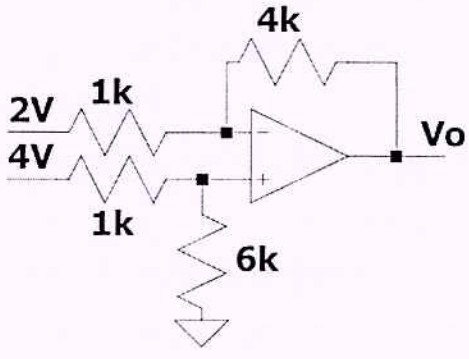
Course Code: ECT301
Course Name: LINEAR INTEGRATED CIRCUITS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	Draw the equivalent circuit of a practical op-amp and list its four non ideal dc characteristics	3
2	A differential amplifier has common mode gain of 0.1 and difference mode gain of 500. Calculate output voltage for input signals V_1=0.7mV and V_2=0.4mV	3
3	Draw a half wave rectifier circuit to rectify an ac voltage of 0.2V. Explain the process of rectifying such a low signal	3
4	Find the output voltage for the circuit shown in figure	3



5	Design RC phase shift oscillator for a frequency of 2kHz	3
6	Design second order butterworth high pass filter with f_L=2kHz	3
7	Draw the block diagram of frequency multiplier using PLL	3
8	Design a monostable multivibrator using 555 timer for a pulse period of 1ms	3
9	What is the significance of the reference voltage supply in IC 723?	3
10	Define the terms (a) Line regulation, (b) Load regulation and (c) Ripple Rejection	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

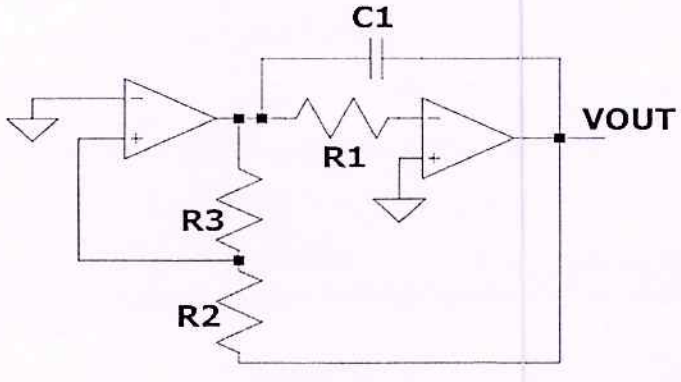
11	a)	Derive expression for differential gain, common mode gain, CMRR and differential input resistance for dual input unbalanced output differential amplifier	7
	b)	Wilson current mirror is superior to normal current mirror. Establish mathematically	7
12	a)	For dual input balanced output differential amplifier R_C=2.2K, R_E=4.7K, Vcc=10V, V_{EE}=10V. For the transistors have β=100 and V=0.7V. Determine (a) Q points (b) Differential voltage gain	10
	b)	An op-amp 741 connected as a unit gain inverting amplifier having a slew rate of 0.5V/μs. Determine the time taken for the output to change by 10V	4

Module -2

13	a)	Explain the op-amp circuit for voltage shunt feedback. Derive the expression for closed loop gain, input resistance and output resistance.	7
	b)	Explain the working of V to I converter with grounded load	7
14	a)	Draw the circuit of instrumentation amplifier. Derive an expression for its differential gain	7
	b)	Design Schmitt trigger for UTP=2V, LTP= -2V	7

Module -3

15	a)	Explain the working of wienbridge oscillator. Derive an expression for frequency of oscillation	7
	b)	Design a square wave oscillator for fo=1kHz using 741 op-amp with dc supply voltage ±12V and duty cycle 50%	7
16	a)	Derive an expression for transfer function of first order LPF	7
	b)	For the circuit shown in figure R_1=100kΩ, R_2=10kΩ, R_3=20kΩ, C_1=0.01μF and ±Vsat=±14V for the op -amps. Determine (a) period, (b) peak value of square wave (c) peak value of triangular wave	7



Module -4

17	a)	Design an astable multivibrator using 555 timer for a frequency of 1kHz and a duty cycle of 70%. Assume C=0.1μF	7
	b)	Draw the block diagram of PLL IC 565 and explain its operation	7
18	a)	Determine the change in control voltage v_c during lock, if input signal frequency f_s= 20kHz , the free running frequency is 21kHz and the V/F transfer coefficient of VCO is 4kHz/V.	7
	b)	Define Capture range, lock range and pull in time of PLL	7

Module -5

19	a)	What is fold back current limiting? Draw a regulator circuit with this implementation	7
	b)	With block diagram describe the working of successive approximation ADC	7
20	a)	Draw the circuit diagram of an n bit weighted resistor DAC. Explain its operation.	7
	b)	A system employs a 16 bit word for representing an input signal. If the maximum output voltage is set to 2V, calculate resolution of the system and its dynamic range	7

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