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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (R,S) Examinations April 2026 (2019 Scheme)

Course Code: ECT312
Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 Discuss the key differences between synchronous and asynchronous sequential circuits. (3)

2 Briefly explain three state assignment methods that can be used in the design of clocked synchronous sequential circuits with examples. (3)

3 Describe the concept of a merger diagram and illustrate it with an example (3)

4 With examples, differentiate between critical and non-critical race conditions in asynchronous sequential circuits. (3)

5 Distinguish between static and dynamic hazards in digital circuit design. (3)

6 Explain the concept of clock skew and mention any two factors responsible for it. (3)

7 Briefly describe any three test pattern generation approaches for BIST. (3)

8 Define Automatic Test Pattern Generation (ATPG). State its purpose and importance in VLSI testing. (3)

9 What is the role of the switch matrix in a CPLD? Explain with reference to the XC9500 family. (3)

10 Describe the role of programmable interconnect in Xilinx XC4000 FPGA family. (3)

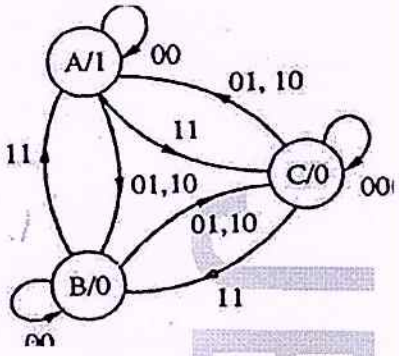
PART B

Answer one full question from each module, each carries 14 marks.

Module I

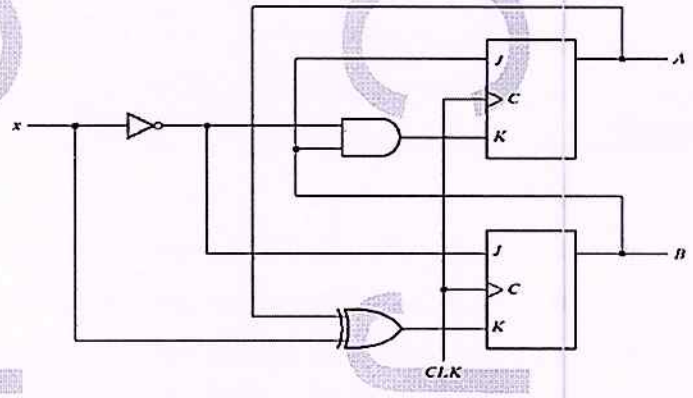
11 a) Design a sequence detector which generates an output z =1, whenever the string is 1101, and generates a '0' at all other times. The overlapping sequences are detected. Implement the Mealy model circuit using D FFs. (9)

b) Construct an ASM chart for the following state diagram shown. (5)



OR

12 a) Analyze the following clocked synchronous sequential network. Construct the excitation table, transition table, state table and state diagram. (7)



b) Using implication chart construct the minimal state table from the state table given below. (7)

PS	X = 0	X = 1	Z
A	G	C	0
B	F	H	0
C	E	D	1
D	A	C	0
E	C	A	1
F	F	B	1
G	A	C	0
H	C	G	1

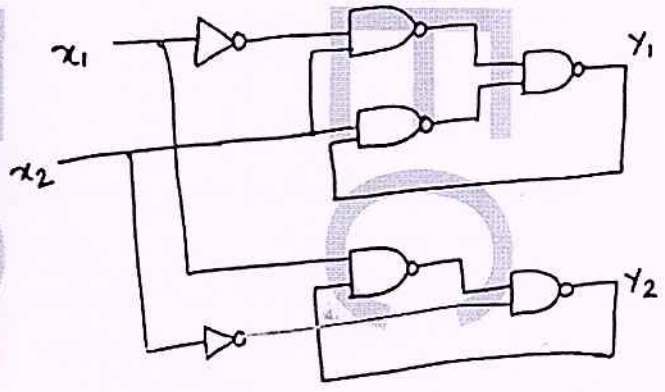
Module II

13 a) Design an asynchronous sequential circuit with two inputs X and Y and an output Z. The output should go high when X = 1 and Y changes from 0 to 1, and stay high until Y returns to 0. (9)

b) Explain any one race free state assignment method in asynchronous sequential network with example. (5)

OR

14 a) Analyze the following asynchronous sequential circuit by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in fundamental mode with the restriction that only one input variable can change value at a time. (8)



b) Obtain the primitive flow table and minimal row flow table for a fundamental mode asynchronous sequential circuit with inputs P and Q and output R. When P = 1, output R should be 1 if Q = 0, and when P = 0, output R should stay constant. (6)

Module III

15 a) Given the SOP expression F=$\sum$ (1,2,3,7), construct the corresponding logic circuit. Analyze the possibility of hazards in the circuit and explain how they can be removed. Draw the hazard free circuit. (9)

b) What is switch bounce? Explain how a debouncing circuit using an SR latch helps to overcome the problem of switch bounce. (5)

OR

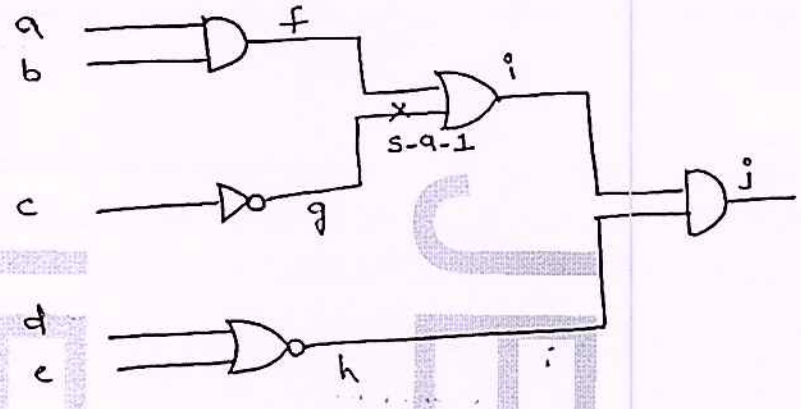
16 a) Analyze the Boolean expression F = w′ x + w x′ y + x y for static-1 hazards. If detected, eliminate them using redundant terms and draw the hazard free circuit. (8)

b) With the help of a neat timing diagram, explain the operation of a two-flip-flop data synchronizer. (6)

Module IV

17 a) Illustrate the fault table method used for effective test set generation for the circuit with the Boolean function F = A B + A′ C. (8)

b) Describe the path sensitization method for fault detection. Using path sensitization, find the test set for the fault SA1 at g in the following circuit. (6)



OR

18 a) Find the test vector of all SA0 and SA1 faults of the circuit whose Boolean function is f = x1 x2 + x1 x3'x4' + x2 x4 by the Kohavi algorithm. (8)

b) Describe the Boolean difference method for detecting faults with an example. (6)

Module V

19 a) Describe the input/output block (IOB) structure in the XC9500 CPLD family and explain how it supports different I/O standards with the help of a diagram. (7)

b) Explain the structure of a configurable logic block (CLB) in the XC4000 FPGA. Discuss how CLBs are used to implement combinational and sequential logic. (7)

OR

20 a) Compare the XC9500 CPLD family with XC4000 FPGA in terms of architecture, flexibility, and typical applications. (6)

b) Describe the architecture of the Xilinx XC4000 FPGA family with the help of a functional block diagram. (8)

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