Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (R,S) (FT/WP/S4PT) Examinations April 2026 (2019 Scheme)

Course Code: ECT304
Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks.

		Marks
1	Differentiate between ASIC and FPGA.	(3)
2	Explain the significance of Moore's law in semiconductor industry.	(3)
3	List the demerits of pass transistor logic.	(3)
4	Realize 2 input XOR gate using static CMOS logic.	(3)
5	Explain the working of a one transistor DRAM memory cell.	(3)
6	Explain the basic principle of operation of dynamic logic.	(3)
7	Write the Propagate, Generate and Delete signals for a full adder circuit.	(3)
8	Compare the delay performance of ripple carry, linear carry select and square root carry select adders.	(3)
9	Compare wet and dry oxidation in fabrication process.	(3)
10	What are the design rules in VLSI chip design?	(3)

PART B

Answer onefull question from each module, each carries 14 marks.

Module I

11	a)	With the help of a flow chart, explain FPGA Design flow.	(8)
	b)	Explain Full custom and standard cell based ASIC designs.	(6)

OR

12	a)	Distinguish between Top down and Bottom up approach.	(10)
	b)	List the advantages of SoC.	(4)

Module II

13	a)	Draw the Voltage transfer characteristics of a static CMOS inverter. Explain the different regions of operation of CMOS inverter.	(10)
	b)	Implement the 4x1 multiplexer using Transmission gates.	(4)

OR

14 a) Why PMOS transistor can pass only strong ones and NMOS can pass strong zeros? (8)

b) Explain switching power dissipations in CMOS logic. (6)

Module III

15 a) Design a 4 × 4 OR-based ROM array and explain its working. (8)

b) Design the circuit of a 3 input NOR gate using dynamic CMOS logic and 3-input OR gate in Domino logic. (6)

OR

16 a) Explain the basic principle of operation of Domino logic. What are its advantages? (7)

b) With a neat circuit diagram, explain the read operation in a 6 transistor static RAM memory. (7)

Module IV

17 a) Design static CMOS full adder cell with not more than 28 transistors using logic level optimisation. (10)

b) Explain the working of a 16-bit linear carry adder with a neat block diagram. (4)

OR

18 a) With neat implementation diagram explain the working of 4*4 array multiplier. (8)

b) Explain the logic of square root carry select adder. (6)

Module V

19 a) Explain the steps involved in photolithography process. (10)

b) What is the difference between stick diagram and layout diagram in VLSI design? (4)

OR

20 a) Explain the manufacturing steps of single crystal Silicon from Quartzite. (10)

b) Draw the stick diagram of a two-input CMOS NAND gate. (4)

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