Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R) Examinations April 2026 (2024 Scheme)

Course Code: PCMRT402
Course Name: DIGITAL ELECTRONICS

Max. Marks: 60 Duration: 2 hours 30 minutes

PART A

(Answer all questions. Each question carries 3 marks)

		CO	Marks
1	Write the Verilog identifiers rules with two examples.	CO1	(3)
2	Subtract using 2's complement method: $110101_2 - 101011_2$	CO1	(3)
3	Obtain the minterms for the Boolean function: F(A,B,C) =A'B+AC	CO2	(3)
4	Identify the logic level characteristics of TTL logic.	CO2	(3)
5	Write the Verilog gate-level code for a Half Adder.	CO3	(3)
6	Design a 1:8 De-Multiplexer and determine which output becomes active when $S_2S_1S_0 = 101$.	CO3	(3)
7	Identify the main advantages of FPGA over PAL	CO4	(3)
8	Derive the characteristic equation of a JK flip-flop.	CO4	(3)

PART B

(Answer any one full question from each module, each question carries 9 marks)

Module -1

9	a)	Write a Verilog module for a 2-input AND gate and explain the use of identifiers, data objects, and operators.	CO1	(5)
	b)	Convert i) $(3A5)_{16}$ to decimal ii) $(645.27)_8$ to hexadecimal	CO1	(4)

10	a)	Explain fixed-point and floating-point representation with suitable numerical examples.	CO1	(6)
	b)	Represent the following decimal numbers in 8-bit signed representation complement and perform the subtraction: (+45) − (23).	CO1	(3)

Module -2

11		Simplify the following Boolean function using the Quine–McCluskey method: $F(A,B,C,D) = \Sigma m(0,1,2,5,6,7,8,9)$	CO2	(9)
12		Explain the internal structure and working of a TTL NAND gate with diagram.	CO2	(9)

Module -3

13	a)	Design a logic circuit using decoder to implement the Boolean function $F(A,B,C) = \Sigma m(1,4,6,7)$.	CO3	(4)
	b)	Write the Verilog declaration for a 4-input multiplexer module.	CO3	(5)
14	a)	Explain the working of a BCD Adder and determine the result for $45 + 38$.	CO3	(9)

Module -4

15	a)	Design a 3 bit synchronous Up counter using JK flipflop.	CO4	(6)
	b)	Explain with a logic diagram a serial in parallel out shift register.	CO4	(3)
16	a)	Explain the working of Johnson counter with timing diagram.	CO4	(6)
	b)	Write the Verilog gate level code for a D flip flop.	CO4	(3)

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