D
00A-1CB97

16PBEET404042601

Pages: 3

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R) (FT/WP) Examinations April 2026 (2024 Scheme)

Course Code: PBEET404
Course Name: DIGITAL ELECTRONICS

Max. Marks: 40 Duration: 2 hours 30 minutes

PART A

(Answer all questions. Each question carries 2 marks)

		CO	Marks
1	Perform the following number conversions i) $(53)_{10}$ to Excess – 3 code ii) $(110010)_2$ to grey code	1	(2)
2	Covert the given equation in standard form f(A,B,C)= $\overline{A}B + B + A\overline{C}$	1	(2)
3	Implement half subtractor using NAND gate	2	(2)
4	Implement f(A,B,C) = $\sum$m(1,3,5,7) using 8 X 1 MUX	2	(2)
5	Differentiate between a sequential circuit and combinational circuit.	2	(2)
6	Draw the characteristic and excitation table of JK Flip flop	3	(2)
7	Compare between Moore & Mealy machine.	3	(2)
8	Write any 4 specifications of ADC (Analog to Digital Converter)	4	(2)

PART B

(Answer any one full question from each module, each question carries 6 marks)

Module -1

			CO	Marks
9	a)	Represent the following decimal numbers using 12-bits in i) sign-magnitude ii) 1's complement and iii) 2's complement forms. a) -21 and b)	1	(4)

-53. Also add the two numbers using 2's complement method.

	b)	Compare the performance of TTL and CMOS	1	(2)
10	a)	Reduce the expression using K map in SOP form and implement using minimum number of NAND gate f(A,B,C,D) =$\sum$ m(6,7,8,10,11,15)+ $\sum$ d(0,2,3,4,5,9,14)	1	(4)
	b)	Draw the internal diagram of CMOS NOR gate	1	(2)

Module -2

11	a)	Implement the following sum of minterms expression using an 8:1 multiplexer. f(A,B,C,D) = $\sum m$(0,1,3,6,12,13,14,15).	2	(4)
	b)	Explain 3 bit parity generator	2	(2)
12	a)	Explain the working of a comparator which can compare two 2-bit binary numbers, A =A_2A_1 and B =B_2B_1 (A_1 *and* B_1 are the LSB and A_2 and B_2 are MSB). Deduce expressions for the outputs when $A > B$, $A < B$, and $A = B$. Implement these expressions using logic gates.	2	(4)
	b)	Derive the equation for sum and carry of a full adder	2	(2)

Module -3

13	a)	Design a MOD 6 asynchronous counter using JK Flip flop and draw the timing diagram	3	(4)
	b)	Draw a three bit ring counter and its timing diagram	2	(2)
14	a)	Design a synchronous counter that count only the states 0,3,4,6,7….	3	(4)
	b)	Draw a 3-bit SISO shift register and its timing diagram	3	(2)

Module -4

15	With the help of a neat circuit diagram, explain how a R-2R ladder type DAC converts a digital signal to analog signal.	4	(6)
16	Explain the working of a flash type analog to digital converter (ADC) with the help of a neat circuit diagram.	4	(6)

***