Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R) Examinations April 2026 (2024 Scheme)

Course Code: PEECT415
Course Name: DIGITAL SYSTEMS AND VLSI DESIGN

Max. Marks: 60 Duration: 2 hours 30 minutes

PART A

(Answer all questions. Each question carries 3 marks)

		CO	Marks
1	Differentiate between Mealy and Moore state machines.	1	(3)
2	Explain the main components in an ASM chart.	1	(3)
3	Differentiate between critical and non-critical races in asynchronous sequential circuit with the aid of an example.	2	(3)
4	List the steps in obtaining flow table from the state table in an asynchronous sequential circuit.	2	(3)
5	Differentiate between clock skew and clock jitter.	3	(3)
6	Draw the architecture of BIST and explain the function of each block.	3	(3)
7	Explain the various data types used in modelling of circuits in VHDL.	4	(3)
8	Write the VHDL code for a JK flip flop with asynchronous reset using behavioural modelling.	4	(3)

PART B

(Answer any one full question from each module, each question carries 9 marks)

Module -1

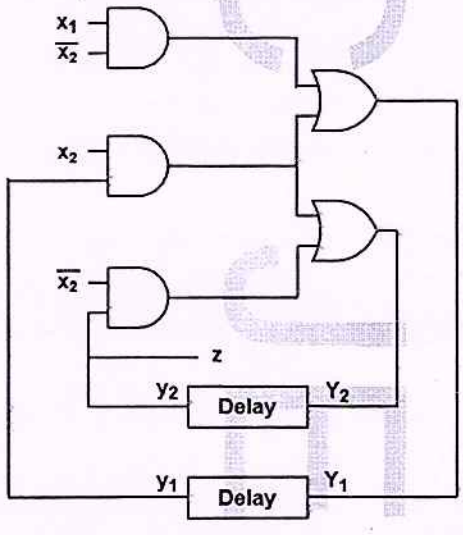
9	Obtain the state transition table for a Mealy CSSN having a single input line x and a single output line z. An output of 1 is to be produced coincident with each third multiple of the input symbol 1. At all other times, the network is to produce 0 as output. An example of the input-output sequence is given below. x = 0 1 1 0 1 0 1 1 1 1 0 0 0 1 1 1 0 z = 0 0 0 0 1 0 0 0 1 0 0 0 0 0 1 0 0	1	(9)

10 Construct the minimal state table from the state table given below using implication chart. 1 (9)

Present State	Next State		Output (z)
	$x=0$	$x=1$	
A	B	C	1
B	D	E	0
C	A	F	1
D	E	C	0
E	G	H	1
F	B	H	1
G	D	F	0
H	F	E	1

Module -2

11 Analyse the asynchronous sequential circuit given below by forming the excitation/transition table, state table, flow table and flow diagram. 2 (9)

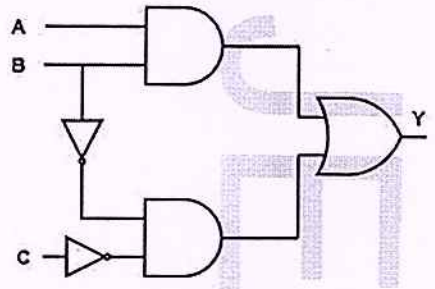


12 Determine a state assignment involving minimum number of variables for the reduced flow table given below. The state assignment should be such that critical races are avoided. Then construct the state transition table. Assign outputs where necessary in such a way that there is at most a single output change during the time the network is unstable. 2 (9)

Present State	Next State				Output (z)			
	Input (x_1x_2) =				Input (x_1x_2) =			
	00	01	10	11	00	01	10	11
A	(A)	(A)	D	(A)	0	0	_	0
B	(B)	A	C	_	1	_	_	_
C	B	(C)	(C)	(C)	_	1	1	1
D	A	-	(D)	C	_	_	0	_

Module -3

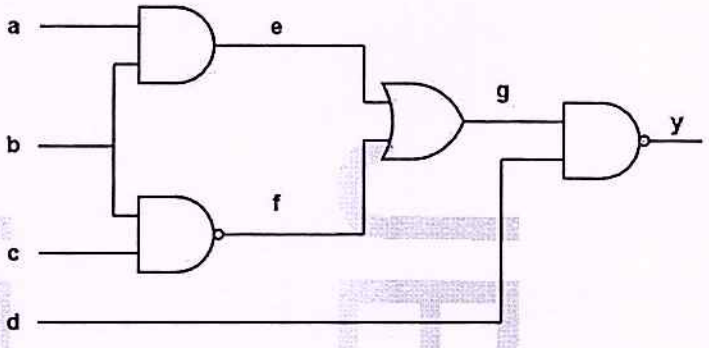
13 For the circuit given below, detect if there is a possibility of hazard. If so, discuss the technique for eliminating the hazard and draw the hazard free realization of the circuit. 3 (9)



14 For the circuit given below, determine the test vector for the following faults using path sensitization method. 3 (9)

(i) SA1 at f

(ii) SA0 at e



Module -4

15 Design the following circuits in VHDL 4 (9)

(i) 2:1 MUX using data flow modelling

(ii) 4:1 MUX using structural modelling

16 Design a Mealy FSM that detects overlapping sequence of 101 in VHDL. 4 (9)

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