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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R) (FT/WP) Examinations April 2026 (2024 Scheme)

Course Code: PBCST404

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE

Max. Marks: 40 Duration: 2 hours 30 minutes

PART A

(Answer all questions. Each question carries 2 marks)

		CO	Marks
1	Differentiate between Big-endian and Little-endian assignment for word addressing, with suitable example.	CO1	(2)
2	Let the content of register S3 in a RISC V machine be - 1111 1111 0001 1100 0001 0000 1110 0111 - show the content of register t3 and t4 after executing the following instructions. **slli t3, s3, 5** **srai t4, s3, 2**	CO1	(2)
3	With suitable examples explain two types of hazards in RISC V pipelined processors.	CO2	(2)
4	Additional pipeline stages allow a processor to go faster, why don't processors have 100 pipeline stages, justify your answer.	CO2	(2)
5	A processor has the following parameters: Cache access time = 1 cycle, Main memory access time = 100 cycles, Cache miss rate = 0.375. Calculate the Average Memory Access Time (AMAT).	CO3	(2)
6	A server performs 2,000 memory accesses, and 1,250 are found in the cache. Calculate the Hit Rate and analyse if this is sufficient for a high-performance environment.	CO3	(2)
7	Analyze the bus arbitration mechanism when the CPU and the DMA controller request access to the system bus at the exact same moment.	CO4	(2)

8		Compare and contrast the sequence of events in a Device-Initiated (Asynchronous) interrupt versus a CPU-Initiated (Synchronous) interrupt.	CO4	(2)

PART B

(Answer any one full question from each module, each question carries 6 marks)

Module -1

9	a)	Translate the following high-level code into RISC-V assembly language. Assume variables a–c are held in registers s0–s2, and f–j are in s3–s7. **// high-level code** //a = b − c; //f = (g + h) − (i + j)	CO1	(3)
	b)	Sketch and explain the instruction execution cycle for RISC V processor.	CO1	(3)
10		Apply your knowledge of RISC-V addressing modes to analyze a set of instructions and determine how operands are accessed in each case. Explain any four addressing modes used, with suitable examples.	CO1	(6)

Module -2

11		Design and explain the datapath operation for the given R type instruction in a single-cycle RISC-V processor. **Address** **Instruction** **Type** 0x1008 or x4, x5, x6 R	CO2	(6)
12	a)	A program containing 100 billion instructions is executed on a RISC-V pipelined processor. The processor has the following characteristics:	CO2	(2)

Average CPI = 1.23

Clock cycle time (T_n) = 350 ps

Answer the following question

1)Calculate the total execution time required to run the program.

2)Briefly explain why the CPI of a pipelined processor is close to 1 but not exactly equal to 1.

b) Illustrate the five stages of a pipelined RISC-V processor with suitable timing diagram and define the function of each stage. CO2 (4)

Also identify the type of hazard(s) (data hazard and/or control hazard) present in the instruction sequence.(Jusify your answer)

I1: lw x5, 0(x1)

I2: add x6, x5, x2

I3: beq x6, x0, LABEL

I4: sub x7, x3, x4

Module -3

13 With neat sketch explain the following cache mapping techniques and analyze their advantages and disadvantages: Direct mapped cache, Set associative cache, Fully associative cache. CO3 6

14 a) What is the primary role of a Translation Lookaside Buffer (TLB) in helping a processor to access memory more quickly. Explain the same using 2-way TLB with neat sketch. CO3 (4)

b) Modern processors use a hierarchy of caches (L1, L2, L3) instead of just one very large L1 cache. Justify your answer. CO3 2

Module -4

15	a)	Evaluate the CPU Utilization levels for Programmed I/O, Interrupt-Driven I/O, and DMA. Which is best for a background file download?	CO4	4
	b)	Define the concept of polling and explain why it is often referred to as "busy waiting" in terms of CPU activity.	CO4	2
16	a)	Why an I/O module is necessary when connecting a GHz-speed CPU to a relatively slow mechanical device like a printer?	CO4	4
	b)	In the context of embedded systems, explain the function and typical use cases of General Purpose I/O (GPIO) and Serial I/O (such as UART or SPI).	CO4	2

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