

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
B.Tech Degree S3 (S) Examinations May 2026 (2024 Scheme)



Course Code: PBECT304
Course Name: LOGIC CIRCUIT DESIGN

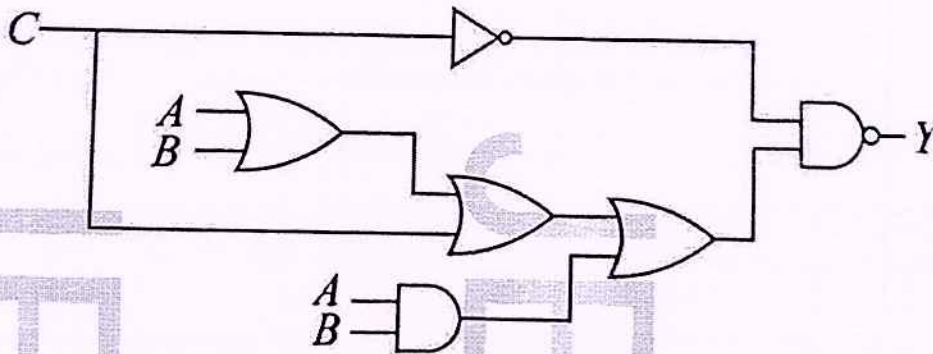
Max. Marks: 40

Duration: 2 hours 30 minutes

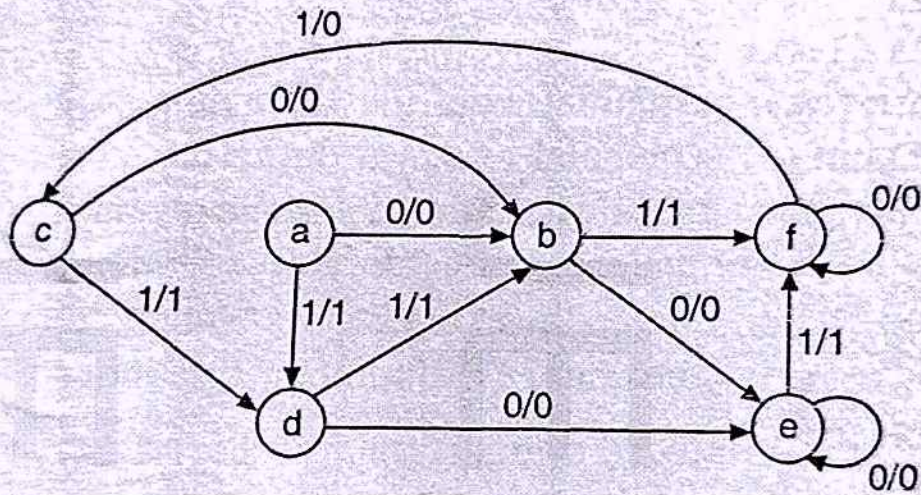
PART A

(Answer all questions. Each question carries 2 marks)

- | | | CO | Marks |
|---|---|----|-------|
| 1 | Obtain the decimal equivalent value of the following numbers.
(i) $FA.FA_{16}$
(ii) 26.24_8 | 1 | (2) |
| 2 | In the logic circuit given in figure below determine the output Y, if the input C is at logic 0. | 1 | (2) |



- | | | | |
|---|---|---|-----|
| 3 | Realize a 4:1 multiplexer using basic gates | 2 | (2) |
| 4 | Write the verilog code to realise a full subtractor based on its logic diagram. | 3 | (2) |
| 5 | Design a sequential circuit to realise an SR flipflop from a D flipflop. | 2 | (2) |
| 6 | Draw the circuit for a SISO shift register using JK flipflop. Briefly explain its working with necessary timing diagrams. | 3 | (2) |
| 7 | Draw the state table and reduced state table for the given state diagram of a Mealy machine | 2 | (2) |



- 8 Briefly explain with a neat circuit diagram the working of a CMOS inverter 4 (2)

PART B

(Answer any one full question from each module, each question carries 6 marks)

Module -1

- 9 a) Determine the sum of two hexadecimal numbers $7F_{16}$ and BA_{16} . Obtain the binary value of the sum and hence convert it from binary to octal. 1 3
- b) Perform the following addition using twos complement number representation 1 3
- (i). $(+13)_{10} + (-2)_{10}$
- (ii). $(-13)_{10} + (+2)_{10}$
- 10 Simplify the following Boolean function together with don't care conditions and express the simplified expression in sum of products form. Realize the resulting expression using NAND gates alone 1 6

$$F(A, B, C, D) = \sum m(4,5,7,12,14,15) + \sum d(3,8,10)$$

Module -2

- 11 a) Design a BCD adder circuit that adds two 4 bit BCD numbers. 2 (3)

- b) Write the verilog code to realize the Boolean function $F1 = \sum m(0,1,2,3,11,12,14,15)$ after minimising it. 3 (3)
- 12 a) Design and realise the Boolean function $F = \sum (1,2,6,7)$ using two 2:1 multiplexers and an external gate. (Assume the multiplexer provides logic high output) 2 (4)
- b) Explain the working of an octal to binary encoder circuit 2 (2)

Module -3

- 13 Design an asynchronous 3 bit up down counter using mode control bit (M), such that the counter counts in the up direction when $M=0$, and in the down direction when $M=1$ using JK flip flops. Draw the timing diagram of the outputs and explain the working of the circuit 2 (6)
- 14 Design a synchronous self starting sequence generator that generates the sequence 0,1,2,4,0,1,2,4,... using D flipflops. 2 (6)

Module -4

- 15 Design a sequence detector using D flipflops, which detects the sequence 1111 permitting overlapping. 2 (6)
- 16 Draw the circuit of a TTL NOT gate and explain its working 4 (6)
