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Pages: 3

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S) Examinations (FT/WP) May 2026 (2024 Scheme)

Course Code: GAEST305

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN

Max. Marks: 60 Duration: 2 hours 30 minutes

PART A

	(Answer all questions. Each question carries 3 marks)	CO	Marks
1	Illustrate the logic function, truth table, logic symbol and waveform representation for the basic gates: AND, OR , XOR.	2	(3)
2	Perform conversion of the following numbers as provided: i) 13AF to Binary ii) $(10110101.101)_2 = (....)_{10}$ iii) $(101101011101)_2 = (...)_{16}$	1	(3)
3	Simplify the given Boolean function and draw the circuit of the given expression using basic gates. F = AB+BC+BC'	2	(3)
4	In a traffic control system modelled using Verilog, the output signal 'go' should turn ON only when both the V input (vehicle detected) and the T input (timer complete) inputs are HIGH (1). Write a Verilog continuous assignment statement to describe this behaviour using a conditional operator.	3	(3)
5	Design a half subtractor and implement it using basic gates.	4	(3)
6	Illustrate the working of a 2 bit One Hot decoder with truth table.	4	(3)
7	Write two short Verilog modules to realize the logic, $Y = A + B.\bar{C}$; one using continuous assignment and another using a procedural block.	5	(3)

8		Design a toggle flip-flop using a JK flip-flop and show how it can be used to divide the clock frequency by two.	5	(3)

PART B

(Answer any one full question from each module, each question carries 9 marks)

Module -1

9	a)	Explain the concept of noise margin in a logic circuit. Using the given DC specifications, calculate the low - level and high-level noise margin. $V_{IL\ max}$ =+2.0 V , $V_{OL\ max}$ =+1.5V , $V_{OH\ min}$ =+2.5 V , $V_{IH\ min}$=+2.5v .	2	(4)
	b)	Illustrate the steps involved in modern digital design flow with proper diagram.	3	(5)
10	a)	How is fixed point number representation different from floating-point number representation? What are the typical applications of these number systems?	1	(4)
	b)	A computer uses 8-bit 2's complement representation for signed numbers. Perform the following operations on A = 55 and B = 85 and express the final result in signed decimal form. a. Perform A – B using 2's complement arithmetic b. Perform A + B using 2's complement arithmetic	1	(5)

Module -2

11	a)	Design a 3 bit Binary to Gray code converter.	4	(5)

	b)	Two continuous assignment statements are used in a Verilog module as shown below:
		assign #2 x = (a && b) ? 1'b1 : 1'b0;
		assign y = !a;
		Explain how these statements together demonstrate concurrent behaviour in
			3	(4)

Verilog. How does the delay element affect the target signals?

12	a)	Simplify the expression by a) considering the don't care condition and b) ignoring the don't care condition. In each case. implement the minimum expression by using logic gates. $Y = \sum m\,(0,1,2,3,4,6,8,10,12,14) + \sum d\,(5,7,10)$.	2	(5)
	b)	Implement the following function using continuous assignment with logical operator in Verilog. $F(A,B,C) = \sum m\,(1,5,7)$.	3	(4)

Module -3

13	a)	Design and implement a two-bit comparator using basic gates.	4	(5)
	b)	Design a full subtractor circuit and write the Verilog code for it using gate level primitives.	4	(4)
14	a)	Design a 8:1 multiplexer using two 4:1 multiplexers	4	(4)
	b)	Derive the Boolean expression for SUM and CARRY outputs for a full adder. Add the binary numbers 1101 and 1011 using full adder logic. Show step by step carry generation.	4	(5)

Module -4

15	a)	Develop a finite state machine to implement a 2-bit up/down counter.	5	(6)
	b)	Write a Verilog code to simulate a D flip-flop.	5	(3)
16	a)	How does an asynchronous ripple counter work? What is the basic principle behind it? Illustrate with suitable logic and timing diagram.	5	(5)
	b)	How is a JK flipflop different from an SR flip flop? Illustrate the difference with the help of truth tables and logic circuits using universal gates.	5	(4)

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