Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (S,FE) (FT/WP/S4 PT) Examination December 2025 (2019 Scheme)

Course Code: ECT304

Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1		Compare Top down and Bottom up approach in VLSI design.	(3)
2		What are ASICs? Explain the different types of ASICs.	(3)
3		List the advantages of CMOS logic.	(3)
4		Explain the implementation of a 2:1 multiplexer using transmission gate logic.	(3)
5		Explain the working of a one transistor DRAM memory cell.	(3)
6		Draw the circuit of a 3 input NOR gate using Dynamic CMOS logic.	(3)
7		Compare the delay performance of ripple carry, linear carry select and square root carry select adders.	(3)
8		List the number of AND gates, half adders and full adders required for implementing a 4*4 array multiplier.	(3)
9		What is meant by design rules in VLSI chip design?	(3)
10		Explain the processes involved in the conversion of raw SiO2 to electronic grade silicon.	(3)

PART B

Answer one full question from each module, each carries 14 marks.

Module I

11	a)	Explain gate array based ASIC design.	(6)
	b)	Draw and explain the internal architecture of SoC. List its applications	(8)

OR

12	a)	Compare ASIC and FPGA	(4)
	b)	With a neat flowchart, explain FPGA design flow.	(10)

Module II

13	a)	Implement a 4x1 multiplexer using Transmission gates.	(4)
	b)	Discuss the different operating regions of a CMOS inverter with relevant equations.	(10)

OR

14	a)	Why PMOS transistor can pass only strong ones and NMOS can pass strong zeros?	(7)
	b)	What are the factors that affect the static and dynamic power dissipations in a CMOS circuit? Derive the total power dissipation of a CMOS circuit.	(7)

Module III

15	a)	Draw the circuit of a 3T DRAM cell and explain read and write operation.	(7)
	b)	Compare Domino logic and NP domino logic.	(7)

OR

16	a)	Implement a 4 x 4 NOR based ROM to store the data 1010,1011, 1001 and 0110.	(7)
	b)	What is Dynamic CMOS logic? Compare static and dynamic CMOS logic.	(7)

Module IV

17	a)	With a diagram, illustrate the principle of operation of an 4X4 array multiplier. Estimate the propagation delay.	(8)
	b)	Explain the working of a 16-bit carry bypass adder with a neat block diagram.	(6)

OR

18	a)	With a neat block diagram, explain the operation of a 16-bit linear carry select adder. Estimate the critical path delay.	(7)
	b)	Explain the working of square root carry select adder. Write down the equation of its critical path delay.	(7)

Module V

19	a)	Explain Twin Tub process with necessary diagrams.	(8)
	b)	Draw the stick diagram and layout of 2 input NOR gate.	(6)

OR

20	a)	Compare photolithography and electron beam lithography.	(8)
	b)	With a neat diagram, explain molecular beam epitaxy.	(6)

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