Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (S,FE) Examination December 2025 (2019 Scheme)

Course Code: ECT312

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each question carries 3 marks. Marks

1		List the State Assignment Rules for obtaining an optimal design.	(3)
2		Draw the state diagram to detect the overlapping Moore sequence 101.	(3)
3		Differentiate a primitive flow table from an ordinary flow table.	(3)
4		What is a race in asynchronous sequential circuits? Briefly explain the two types of races.	(3)
5		Write a short note on Jitter.	(3)
6		Explain Dynamic Hazards with an e.g.	(3)
7		What is the principle of Path sensitization method and mention its advnatages.	(3)
8		List the 3 restrictions imposed on networks for applying the Kohavi's Algorithm.	(3)
9		What are the advantages of FPGA?	(3)
10		Write a note on Programmable Interconnects.	(3)

PART B

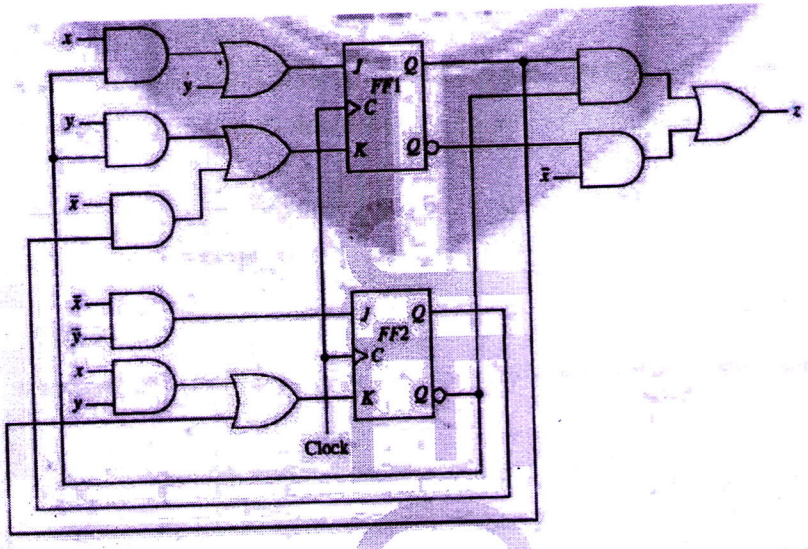
Answer one full question from each module, each question carries 14 marks.

Module I

11	a)	Design a clocked synchronous Serial Binary Adder using Moore model using D flip-flop for realization.	(8)
	b)	Analyse the general components of an ASM block with the aid of well labelled diagrams.	(6)

OR

12	a)	Analyse the following CSSN and derive the next state and output equations. Obtain the excitation table, transition table, state table and state diagram.	(8)



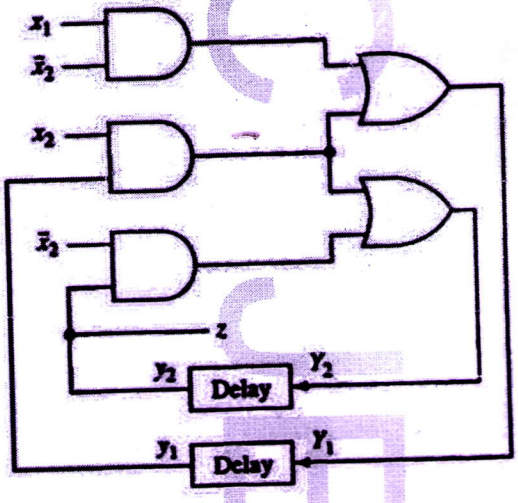
b) Obtain a minimal state table for a clocked synchronous sequential network having a single input line 'x' in which the symbols 0 and 1 are applied and a single output line 'z'. An output of 1 is to be produced if and only if the 3 input symbols following two consecutive input 0's consist of at least one 1. An example of input/output sequences that satisfy the conditions of the network specifications is: (6)

x= 0100010010010010000000011

z= 0000001000000100000000001

Module II

13 a) Analyse the asynchronous sequential network given below by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in the fundamental mode with the restriction that only one input variable can change at a time. (9)



b) Explain in detail the design of an ALU. (5)

OR

14 a) Design a fundamental mode asynchronous sequential circuit with two inputs x1 and x2 and with one output z. Whenever x2 is '1' input x1 is transferred to z. When x2 is '0' the output data does not change for any change in x1. (9)

b) Explain any one race free state assignment method in asynchronous sequential network with example. (5)

Module III

15 a) Examine the possibility of hazard in the AND- OR logic circuit whose Boolean function is given by f(x1, x2, x3)= π(0,1,2,6). Show that there is a static 0 hazard when x1 and x2 are equal to 0 and x2 goes from 0 to 1. Draw the hazard free circuit. (8)

b) Describe the operation of mixed operating mode (MOM) asynchronous sequential circuit with the aid of standard model. (6)

OR

16 a) Draw the logic diagram of the POS expression Y= (x1+x2') (x2+x3). Show that there is a static-0 hazard when x1 and x3 are equal to 0 and x2 goes from 0 to 1. Find a way to remove the hazard by adding one or more gates (8)

b) Explain clock skew? Differentiate between positive and negative clock skew. (6)

Module IV

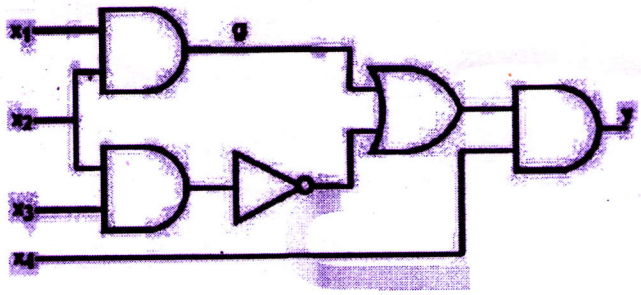
17 a) What is a fault? How are faults classified? Define the terms: fault detection, fault location, test vector, Essential test vector, selective test vector and minimal complete test set. Explain the steps involved in the testing process. (8)

b) Draw the logic diagram for the expression f = $(x_1x_2+x_3')(x_3+x_4)$. Find the test vectors for detecting the faults at input line, x_3 using Boolean difference method. (6)

OR

18 a) For the circuit given in figure below, find the test vectors for the following faults using path sensitization method. (7)

(i) SA0 at x3 (ii) SA1 at x3 (iii)SA0 at g (iv) SA1 at g.



b) Find the test vectors for all SA0 and SA1 faults in the circuit whose Boolean function is $f= x_1x_2+x_2'x_3+x_3x_4'$ using Kohavi's algorithm. (7)

Module V

19 a) Explain the architecture of XC 4000 FPGA family. (7)

b) With suitable sketches, describe the internal structure of XC4000 Configurable Logic Block (CLB). (7)

OR

20 Draw and explain the features of architecture of Xilinx 9500 CPLD family. Also explain the function block, input-output block and switch matrix architecture. (14)

****