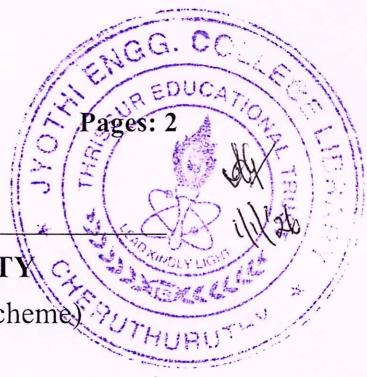


Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
 B.Tech Degree S3 (S,FE) Examination December 2025 (2019 Scheme)



**Course Code: RAT205**

**Course Name: DIGITAL ELECTRONICS**

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer all questions. Each question carries 3 marks*

Marks

1	What are Gray codes? Convert Binary number 110010 into Gray code.	(3)
2	Define any three characteristics of a digital IC.	(3)
3	Prove that $A + A' B = A + B$	(3)
4	Develop a truth table for the standard SOP expression $A'B'C + AB'C' + ABC$ .	(3)
5	Differentiate flip flop and latch.	(3)
6	What do you mean by Decade counter? A decade counter is applied with a frequency of 10 MHz .Find its output frequency	(3)
7	What is the use of a D/ A Converter? What are the two types of DAC?	(3)
8	What do you mean by Resolution and linearity of a DAC counter?	(3)
9	Explain the basic memory operations.	(3)
10	Write the verilog code for NOR gate.	(3)

**PART B**

*Answer any one full question from each module. Each question carries 14 marks*

**Module 1**

11	a	Determine the binary, hexadecimal and octal conversions of (i) 87.15625 (ii) 172.25 (iii) 284	(9)
	b	What are universal gates? Why are they called so? Realise basic gates using any one universal gate.	(5)
12	a	Draw the circuit diagram of TTL NAND and explain its operation.	(8)
	b	Compare TTL and CMOS logic families.	(6)

**Module 2**

13	a	Simplify the logic function $F(A,B,C,D) = \sum m(6,7,8,10,11,15) + d(0,2,3,4,5,9,14)$ using K map in SOP form and implement using NAND gates only.	(8)
	b	Explain the working of a ripple carry adder using an example.	(6)
14	a	Design a full subtractor. Implement full subtractor using two half subtractors.	(10)
	b	Differentiate between multiplexer and demultiplexer.	(4)

**Module 3**

15 a Implement the conversion of SR Flipflop to JK Flip flop. (7)  
b Explain the operation of a master slave JK flip flop. (7)

16 a Explain the operation of parallel in serial out shift register. (7)  
b Design a mod 5 asynchronous counter using JK flip flop. Show the timing diagram. (7)

**Module 4**

17 a Explain the working of successive approximation ADC with an example. (10)  
b Draw the timing diagram of a 4 bit ring counter. (4)

18 Design a 3 bit synchronous up-down counter using T flip-flops. (14)

**Module 5**

19 Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle. (14)

20 a Write the Verilog code for full subtractor. (4)  
b Explain the concept and working of PLA. Compare PLA and PAL. (10)

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