

**SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE
EXAMINATION, JUNE 2010**

IT 04 604—COMPUTER ARCHITECTURE

(2004 Admissions)

Time : Three Hours

Maximum : 100 Marks

Answer all questions.

- I. (a) Write the code sequence for $A = B + C * D$ for the four classes Instruction set.
 (b) What are the different ways of interpreting memory address ? Explain using examples.
 (c) Define Ideal pipeline CPI. What are the techniques that are used to reduce the overall CPI ?
 (d) Using an example, explain register renaming eliminates WAR and WAW hazards.
 (e) Write the steps involved in designing an I/O system.
 (f) What are the different ways of placing a block in a cache ? Explain.
 (g) Write the code for a simple barrier and explain its use in synchronization operation.
 (h) Give the expression for Latency of a message and define each component of the expression.
(8 × 5 = 40 marks)
- II. (a) Explain the five stages of Instruction pipelining using a diagram. (15 marks)
 Or
 (b) (i) Explain the tasks of a computer designer. (8 marks)
 (ii) Explain the various optimization techniques used in a compiler. (7 marks)
- III. (a) (i) Draw the basic structure of MIPS floating point unit using Tomasulots algorithms and explain its operation. (8 marks)
 (ii) Explain how Dynamic scheduling improves the performance in a multiple issue processor. (7 marks)
 Or
 (b) (i) With the help of a diagram, explain the architecture of a vector processor. (9 marks)
 (ii) What are tournament predictor ? What are its advantages ? (6 marks)
- IV. (a) Explain the various techniques used for reducing miss rate. (15 marks)
 Or
 (b) Explain how RAID improves both dependability and performance of storage system. (15 marks)

Turn over

V. (a) What are the solutions for routing in switched media networks ? Explain each solution in detail.

(15 marks)

Or

(b) (i) Explain how synchronization is done in distributed shared memory systems. (8 marks)

(ii) Compare shared and switched media. (7 marks)

[4 x 15 = 60 marks]

Answer all questions.

(a) Write the code sequence for A = B + C * D for the four classes instruction set.

(b) What are the different ways of interrupting memory address ? Explain using examples.

(c) Define ideal pipeline CPI. What are the techniques that are used to reduce the overall CPI ?

(d) Using an example, explain register renaming eliminates WAR and WAW hazards.

(e) Write the steps involved in designing an IO system.

(f) What are the different ways of placing a block in a cache ? Explain.

(g) Write the code for a single barrier and explain its use in synchronization operation.

(h) Give the expression for latency of a message and define each component of the expression.

(8 x 5 = 40 marks)

(15 marks)

(a) Explain the five stages of instruction pipelining using a diagram.

Or

(8 marks)

(b) Explain the tasks of a computer designer.

(7 marks)

(ii) Explain the various optimization techniques used in a compiler.

(a) Draw the basic structure of MIPS floating point unit using Tomasulo's algorithm and explain its operation.

(8 marks)

(ii) Explain how Dynamic scheduling improves the performance in a multiple issue processor.

(7 marks)

Or

(9 marks)

(b) With the help of a diagram, explain the architecture of a vector processor.

(6 marks)

(ii) What are tournament predictor ? What are its advantages ?

(15 marks)

(a) Explain the various techniques used for reducing miss rate.

Or

(b) Explain how RAID improves both dependability and performance of storage system.

(15 marks)

Turn over