D
00J-3GQY1

0200EET206042501

Pages: 2

Reg No.:_______________ Name:__________________________

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S,FE) (FT/WP) (S2 PT) Examination December 2025/January 2026 (2019 Scheme)

Course Code: EET206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	What is ASCII Code?	(3)
2	Which are the universal gates and why are they called so?	(3)
3	State the Principle of Duality with reference to Boolean algebra. Give an example.	(3)
4	Simplify the following Boolean Expression $Y = AB + \overline{AC} + A\bar{B}C\ (AB + C)$	(3)
5	Design a 1-bit magnitude comparator circuit.	(3)
6	What is an ALU?	(3)
7	List any 3 methods to eliminate race around condition in JK flip-flops?	(3)
8	Draw the circuit of a 3-bit Johnson counter.	(3)
9	What is FPGA?	(3)
10	List out 3 specifications of ADC.	(3)

PART B

(Answer one full question from each module, each question carries 14 marks)

Module - 1

11 a) Find the (7)

- i) octal equivalent of $(2F.C4)_{16}$
- ii) binary equivalent of $(374.26)_8$
- iii) hexadecimal equivalent of $(82.25)_{10}$
- iv) decimal equivalent of $(10001110)_2$
- v) excess 3 code of 237

b) Explain fixed-point and floating-point representation of storing real numbers with example. (7)

12 a) Describe the working of CMOS NOR gate with a neat circuit diagram. (7)

b) Determine the value of -39 + 81 using 1's Complement and 2's Complement method of subtraction. Use 8-bit representation including sign bit. (7)

Module - 2

13 a) Explain 4-bit Carry Look Ahead Adder. (9)

b) Implement the following expression using only NOR Gates (5)

$Y = A\overline{B} + B\overline{C} + ABC$

14 a) Design a full subtractor circuit. (8)

b) With the help of K Map, reduce the following expression and implement it. (6)

F (A,B,C,D) = $\sum$ m (0,3,4,5, 7) + d (8, 9, 10, 11, 12, 13, 14, 15)

Module - 3

15 a) What is a parity generator? Design an odd parity generator for a 3-bit message. (9)

b) Use 8 x 1 MUX to implement the logic function $f = A \oplus B \oplus C$. (5)

16 a) Design a circuit to convert a 3-bit Binary to Grey Code. (8)

b) Explain in detail BCD to decimal decoder. (6)

Module - 4

17 a) Draw the characteristic table of J-K flip-flop and excitation table of D flip-flop. Hence, convert a D flip-flop to J-K flip-flop. (7)

b) Design an asynchronous decade counter using J-K flip-flops. Also draw the timing diagrams. (7)

18 a) Design a 2-bit synchronous up/down counter using J-K flip-flops. (8)

b) Explain the working of a 4-bit SISO shift register using D flip-flops with necessary timing diagrams. (6)

Module - 5

19 a) Implement the following using a Verilog program

i) AND Gate (7)

ii) Full Adder

b) Compare Moore and Mealy Circuit with block diagram. (7)

20 a) Explain the working of 3-bit R-2R Ladder type of DAC. (7)

b) Compare PLA and PAL with example. (7)

***