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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S,FE) (FT/WP) (S2 PT) Examination December 2025/January 2026 (2019 Scheme)

Course Code: ECT206
Course Name: COMPUTER ARCHITECTURE AND MICROCONTROLLERS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	During a memory read operation, describe the roles of the address bus, data bus, and control bus and how they coordinate to complete the transfer.	3
2	Distinguish between fixed-point and floating-point representations with examples.	3
3	Identify the addressing mode used in each instruction and justify your choice: (i) MOV A, 30H (ii) MOV A, @R1 (iii) MOVC A, @A+DPTR	3
4	State the functions of EA, PSEN, and ALE pins in the 8051 and mention when each is active/used.	3
5	Write an assembly language code to blink an LED on P1.2 in 8051 using a delay.	3
6	Explain the full-step excitation sequence for a unipolar stepper motor using four control lines.	3
7	Outline how the 8051 derives baud rate using Timer1.	3
8	Explain how the C/T bit selects timer or counter operation.	3
9	Define paging and state its purpose in virtual memory.	3
10	Compare DRAM and SRAM in terms of storage mechanism, refresh requirement and speed.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Show the step-by-step binary division of −8 by +3 using division algorithm. Present the algorithm and the flowchart.	10
	b)	Describe the program counter (PC) and stack pointer (SP) and their roles in a CPU.	4
12	a)	Use Booth's algorithm to compute (−9) × (+7). Show every iteration, include a	10

flowchart, and report the final product in binary and decimal.

b) Differentiate RISC and CISC architectures. 4

Module -2

13 a) Identify the byte range that is bit-addressable in internal RAM and name two bit-addressable SFRs. For byte address 2AH, write the bit addresses of bit5 and bit0 and show how to set/clear them with instructions. 8

b) Consider the following instructions 6

MOV A, #5DH

ADD A, #0A7H

SUBB A, #3BH

Predict the values of CY, AC, OV, P after each operation. Explain how the instructions affect the PSW bits.

14 a) Explain how interrupts are handled in 8051. List the special function registers associated with interrupts and give the significance of each bit. 8

b) Why does 8051 Port-0 require external pull-ups while Ports 1–3 do not? For each port group, state the pin condition when the latch bit is '1' and when it is '0' (assume GPIO mode, no external memory). 6

Module -3

15 a) Write an 8051 assembly language program to find the largest number in a list of 10 unsigned 8-bit numbers stored from internal RAM locations 30H onwards. Store the result in 3AH. 8

b) Explain the initialization sequence and control signals (RS, RW, E) required to interface a 16×2 LCD module with the 8051 in 8-bit mode. Illustrate how the 8051 writes a character to the LCD data register. 6

16 a) Write an 8051 C program to display the decimal digits 0–9 sequentially on a common-cathode 7-segment display interfaced to Port 2. Use an appropriate lookup table for segment codes and provide a software delay between digits. 8

b) With the help of neat block diagrams, explain the interfacing of a matrix keyboard with the 8051. Describe the roles of row/column scanning for the keyboard. 6

Module -4

17 a) Explain the different modes of operation of 8051 timers/counters (Mode 0, Mode 1, Mode 2, Mode 3). For each mode, state the bit settings in TMOD. 8

	b)	Write an 8051 C program to transmit the string "ECT206 CAM" serially at 9600 baud, 8-bit data, 1 stop bit, no parity.	6
18	a)	Describe the serial port SFRs of the 8051. Explain the functions of SCON, SBUF and PCON registers. Briefly discuss how baud rate is controlled using Timer 1.	6
	b)	Describe the steps and calculate the initial values to be loaded into TH0 and TL0 for a delay routine of 10 ms for an 8051 with a 12 MHz crystal using Timer 0 in Mode 1.	8

Module -5

19	a)	Explain programmed I/O and interrupt driven I/O for data transfer in computers.	7
	b)	What is DMA? Explain the role of DMA controller in data transfer using a block diagram.	7
20	a)	Explain computer memory hierarchy. Specify how the various levels in the hierarchy vary.	7
	b)	Explain associative mapping of cache memory for an 8K cache with block size 64 and word size 32. Draw the necessary figures. Specify the main memory address format.	7

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