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Pages: 3

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S,FE) (FT/WP) (S2 PT) Examination December 2025/January 2026 (2019 Scheme)

Course Code: CST202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	Differentiate between big endian and little endian byte ordering with help of examples	3
2	Is there any difference in the updating of program counter register while executing a branch instruction when compared to that during sequential instruction execution? Explain with examples.	3
3	Define Register Transfer Logic (RTL). Show the equivalent hardware implementation of RTL statement $x'T_1: A \leftarrow B$.	3
4	Illustrate with examples, how the carry bit and overflow bit in a status register associated with an 8bit ALU can be set or reset.	3
5	Explain how an array multiplier can increase the efficiency of performing multiplication operations? Find out the number of AND gates and type and number of adders required for constructing a 4x4 array multiplier	3
6	Differentiate between arithmetic pipelines and instruction pipelines.	3
7	Illustrate any two types of control organization.	3
8	List the functionalities provided by a microprogram sequencer.	3
9	Predict how many 512K X 8 memory chips are required to construct 8M X 32 memory?	3
10	List the actions performed by the processor once it receives an interrupt signal.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	What information does the addressing mode give in an instruction? List and explain any 6 addressing modes with examples.	7
	b)	Illustrate a possible arrangement of different components inside the processor using a single bus. Write the complete sequence of control steps for the following operation while using this arrangement.	7

Add #NUM, R1 (Add the immediate number NUM to register R1 and store result to R1)

Assume that the instruction consists of two words The first word specifies the operation and addressing mode. Second word contains the operands.

OR

12 a) Differentiate among one address, two address and three address instructions using examples. 7

Write a program that can evaluate the expression $X = (A+B)x(C+D)$ for a processor that uses two address instructions. The processor has the instructions Load, Store, Multiply and Add.

b) List the advantages of using a multiple bus system. Design a multiple bus system using 3 buses. 7

Module -2

13 a) Design an Arithmetic circuit which can perform 8 arithmetic operation according to the following function table. Assume a 4 bit ALU and two selection variables S_1 and S_0. Input carry C_{in} also determines the operation performed. Draw the circuit diagram for one stage of the designed arithmetic circuit. 10

S_1	S_0	$C_{in}=1$	$C_{in}=0$
0	0	F=A	F=A+1
0	1	F=A+B	F=A+B+1
1	0	F=A+B'	F=A+B'+1
1	1	F=A-1	F=A

b) Illustrate and explain the organization of a processor unit using scratch pad memory. 4

OR

14 a) Draw and explain the block diagram of a processor unit with seven registers, an ALU, shifter and a status register. If the processor has 16 control variables, show how the control word can be derived for the processor. 7

b) Outline the uses of an accumulator in a processor unit. 7

Consider an accumulator with n stages and n flipflops, $A_1, A_2, ... A_n$, with the microoperations controlled by control variables p_j, j=1,2,3... .Illustrate the design procedure for the following logic microoperations in the accumulator.

Control Variable	Micro Operation	Name
p_4	$A \leftarrow A \wedge B$	AND

p_5	A←A V B	OR
p_6	A ←A ⊕ B	Exclusive OR

Module -3

15 a) Outline the restoring method of division for Binary numbers with the help of a flow chart. Illustrate the process by showing the contents of different registers during the division of **10100011 by 1011** 7

b) Explain the concept of arithmetic pipeline with an example? 7

OR

16 a) Illustrate the hardware required and the process for Booth's Multiplication using diagrams and flowchart. Show the process and contents of registers during the multiplication of **(-15)x(-13).** Assume 5 bit registers are used. 7

b) List and explain the three classes of data dependent pipe line hazards and the possible resolutions for these. 7

Module -4

17 a) Explain with help of a diagram , the organization of a microprogrammed CPU. 7

b) What is a microinstruction? Differentiate between horizontal and vertical microinstructions. 7

OR

18 Illustrate the complete set of steps, with appropriate diagrams and tables, for designing a hardwired control circuit for the addition and subtraction of binary numbers in sign magnitude form. 14

Module -5

19 a) Outline any three methods for interrupt handling in a scenario where multiple devices can raise interrupts at the same time. 7

b) A computer system uses 32-bit memory addresses and it has a main memory consisting of 1G bytes. It has a 4K-byte cache organized in the set-associative manner, with 4 blocks per set and 64 bytes per block. Calculate the number of bits in each of the Tag, Set, and Word fields of the main memory address. 7

OR

20 a) Outline the basic architecture of Static RAM and Dynamic RAM using diagrams. Discuss if static RAMs are better than Dynamic RAMs. Justify your opinion with valid reasons. 7

b) Illustrate the concept of Direct memory access and the registers used for that. 7

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