Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (R) (FT/WP) Examination November 2025 (2024 Scheme)

Course Code: PBECT304

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 40 Duration: 2 hours 30 minutes

PART A

(Answer all questions. Each question carries 2 marks)

		CO	Marks
1	Convert $(11001.11)_2$ to octal and decimal number systems	1	(2)
2	Simplify $Y = A + \overline{A} + AB + BC$ using Boolean algebra	1	(2)
3	Write notes on priority encoder	1	(2)
4	Give Verilog code for a Half Subtractor	2	(2)
5	Draw the circuit diagram of a 4-bit Ring Counter	2	(2)
6	Convert a JK flip flop to D and T flip-flops	3	(2)
7	Differentiate Moore and Mealy machines	4	(2)
8	Write notes on Emitter Coupled Logic (ECL)	4	(2)

PART B

(Answer any one full question from each module, each question carries 6 marks)

Module -1

			CO	Marks
9	a)	Simplify the logic function using K – map $y=\sum m(0,1,4,5)$ and realize using NOR gates	3	(3)
	b)	Subtract $(12)_{10}$ from $(68)_{10}$ using 1's and 2's complement arithmetic	2	(3)

10	Suppose a logic circuit has four inputs A, B,C,D. A four-bit input is fed with D as LSB and A as MSB. Design a circuit such that the output is one when the input is more or equal to decimal 6.	2	(6)

Module -2

11	Design a full Adder using NAND gates only.	2	(6)
12	Write notes on carry look ahead adders	2	(6)

Module -3

13	What is race around condition? How it can be eliminated?	3	(6)
14	Design a Mod12 synchronous up counter using T flipflops with necessary diagrams	3	(6)

Module -4

15	Define i) fan in ii) fan out iii) Noise margin iv) Propagation delay	4	(6)
16	Describe the working of 2 input TTL NAND gate with necessary diagram	4	(6)

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