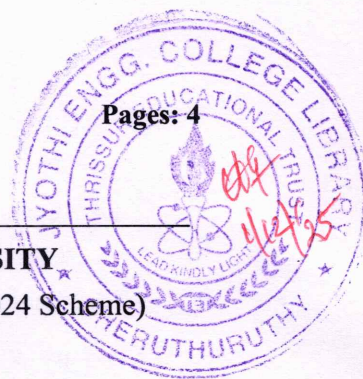


Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

B.Tech Degree S3 (R) (FT/WP) Examination November 2025 (2024 Scheme)

**Course Code: GAEST305****Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN**

Max. Marks: 60

Duration: 2 hours 30 minutes

**PART A***(Answer all questions. Each question carries 3 marks)*

		CO	Marks
1	Perform the following number conversions: i. Binary equivalent of the decimal number, 39.625 ii. Decimal equivalent of the hexadecimal number, A3.B2	1	(3)
2	Illustrate modern digital design flow used in Verilog-based system design with the help of a flowchart.	3	(3)
3	A security system activates an alarm (output = 1) only when exactly two of the three sensors - Door sensor (A), Window sensor (B), and Motion sensor (C) - are triggered. Derive the Boolean expression for the alarm output in terms of A, B, and C. Draw the logic circuit diagram for the same.	2	(3)
4	In a circuit controlling a heating element, the output signal H (heater on) should become 1 only when the input T (temp low) is 1 and the input E (system enable) is 1. However, due to hardware constraints, the output should turn on only after a delay of 5 time units once the condition becomes true. Write a Verilog continuous assignment statement to model this behaviour using a logical operator and a propagation delay.	3	(3)
5	Illustrate the working of a 4 to 2 binary encoder and derive the logic expression for its outputs.	4	(3)
6	Using gate-level primitives, write the Verilog code segment to implement	4	(3)



an XOR gate using only NAND gates.

- |   |   |   |     |
|---|---|---|-----|
| 7 | List the building blocks required for implementing an FSM. Explain how a Moore machine is different from a Mealy machine and illustrate this difference using a suitable block diagram. | 5 | (3) |
| 8 | Write a Verilog behavioural model using a procedural assignment to implement a 2-input AND gate. Draw the output waveform for all input combinations.                                   | 5 | (3) |

### PART B

*(Answer any one full question from each module, each question carries 9 marks)*

#### Module -1

- |    |   |   |     |
|----|---|---|-----|
| 9  | a) Compare the fixed-point and floating-point number systems. Describe how the range and precision of numbers vary between them, and give one suitable example for each representation.   | 1 | (5) |
|    | b) Describe the meaning of logic levels and noise margins in a digital circuit. What are the roles of logic levels and noise margins in ensuring reliable circuit operation?  | 2 | (4) |
| 10 | a) A computer uses 8-bit 2's complement representation for signed numbers. Perform the following operations on $A = 85$ and $B = 55$ and express the final result in signed decimal form.<br><br><div style="margin-left: 40px;"> a. Perform <math>A - B</math> using 2's complement arithmetic<br/> b. Perform <math>A + B</math> using 2's complement arithmetic </div> | 1 | (5) |
|    | b) Define the term "fan-out" in digital circuits. Interpret how driving resistive loads or driving other gates can affect the output performance of a logic gate.   | 2 | (4) |

#### Module -2

- |    |   |   |     |
|----|---|---|-----|
| 11 | a) Construct the truth table showing the conversion from BCD input (A,B,C,D) to Excess-3 output (W,X,Y,Z). Draw the logic circuit diagram | 2 | (5) |
|----|---|---|-----|



implementing the converter using minimum number of basic logic gates.

- b) Simplify the expression using De-Morgans law. 2 (4)

$$F = \overline{\overline{(A+B)} \overline{(B+C+D)} \overline{AC}}$$

- 12 a) A logic function is defined by the following minterms:  $F(A, B, C) = \Sigma m(1, 2, 5, 7)$ . Express the function F in its canonical Product-of-Sums (POS) form. Simplify the expression obtained either using Boolean theorems or by using Karnaugh Maps. Write the function F in canonical Sum-of-Products (SOP) form also. 2 (5)
- b) Write a Verilog continuous assignment to convert a 4-bit binary input (b3,b2,b1,b0) into its Gray code output (g3,g2,g1,g0) using continuous assignment with logical or conditional operators. 3 (4)

### Module -3

- 13 a) A 7-segment display is to show digits 0–7 using a BCD to 7-segment decoder. Show the input-output mapping for the display segments and derive the logic expression for the activation of each segment. Draw the logic diagram of the circuit. 4 (5)
- b) Demonstrate how a 4-to-1 multiplexer can be used to implement the function,  $F(A, B, C) = \Sigma(0, 3, 6, 7)$  when A and B are used as select lines. 4 (4)
- 14 a) Implement a full adder using two half adders. Show all intermediate outputs and derive the final Boolean expressions for Sum and Carry. 4 (4)
- b) Two temperature sensors  $S_1$  and  $S_2$  generate 2-bit values representing measured temperatures. Design a circuit to compare the outputs of these sensors and generate the following control signals: 4 (5)

If  $S_1 > S_2$  : activate Cooling Fan

If  $S_1 < S_2$  : activate Heater

Otherwise: Cooling fan and Heater are inactive.



Derive the Boolean expressions for outputs and draw the logic diagram of the circuit.

#### Module -4

- 15 a) Explain the working of a serial in serial out (SISO) and a serial in parallel out (SIPO) shift register with the help of logic diagrams and timing diagrams for the input 1101. 5 (4)
- b) Design a Moore-type FSM that outputs logic HIGH when three consecutive 1's are detected on the input. Provide the state diagram, state transition table and logic expression for the next state logic. 5 (5)
- 16 a) Design a mod-6 synchronous counter either using JK flip-flops or using FSM design process and D flip-flops. Show the state diagram, state transition table and logic equations to the flip-flop input. 5 (5)
- b) Model a D flip-flop with enable input using behavioural Verilog code. The output should change only when the clock edge occurs and enable = 1. Provide the Verilog code and a short timing explanation. 5 (4)

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