D 10050 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2010

CS/IT 09 306/PTCS 09 305—SWITCHING THEORY AND LOGIC DESIGN

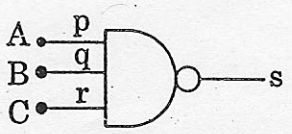
(2009 Admissions)

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*
Each question carries 2 *marks.*

1. Convert $(2142.53)_{10}$ to Octal and binary numbers.
2. Draw the logic diagram of a half adder and form the truth table.
3. Compare combinational and sequential circuits.
4. Determine a complete test set for the 3-input NAND gate as shown below :



5. With neat sketches and truth table explain about negative edge triggered D flip-flop.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*
Each question carries 5 *marks.*

6. State and prove De Morgan's theorems.
7. Implement the logic function

   $Y = \Sigma m (0, 1, 2, 4, 6, 9, 12, 14)$

   using 8 : 1 multiplexer.
8. Explain why NAND and NOR are called universal gates.
9. With a neat block diagram explain signature analysis.
10. What is meant by race around condition ? How can it be avoided ?
11. Show how SR flip-flop is converted to JK and D flip-flops.

(4 × 5 = 20 marks)

Part C

12. (a) Minimize the following functions using K-map :—

    (i) $F(A, B, C, D) = \Sigma m (5, 7, 8, 10, 13, 15) + \Sigma d (0, 1, 2, 3)$.

    (ii) $Y = \pi m (0, 1, 4, 5, 6, 8, 9, 12, 13, 14)$.

Or

Turn over

(b) Using Quine Mc Cluskey method minimize the following function —

$F(A, B, C, D, E) = \Sigma m (0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$.

13. (a) Implement full subtractor using demultiplexer.

Or

(b) Design a code converter combinational circuit to convert binary to BCD.

14. (a) Write notes on PLA minimization.

Or

(b) Explain Boolean difference method for fault detection.

15. (a) Design Mod-10 counter using JK flip-flops and discuss.

Or

(b) Explain different types of shift register counters in detail.

(4 × 10 = 40 marks)