Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S,FE) Examination May 2025 (2019 Scheme)

Course Code: RAT205

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1 What do you meant by Current sinking and Current Sourcing in a TTL Circuit. (3)

2 Represent 3582_{10}. (a). In Octal (b). In Hexadecimal (c). In Excess three code. (3)

3 Design a circuit that will find 2's complement of four bit binary number. (3)

4 Realize a half adder using NOR gates only (3)

5 What is a Register. What are the basic types of shift registers. (3)

6 Explain how a D Flip-Flop is converted to SR Flip-Flop (3)

7 What do you meant by a Offset voltage, accuracy and resolution of D/A Converter. (3)

8 A 6-bit DAC has a full – scale output of 2 mA and a full-scale error of ± 0.5 %. What is the range of possible outputs for an input of 100000? (3)

9 Show that $(A + B)\acute{A}B$ is equivalent to A Ex-OR B. Construct the corresponding logic diagrams. (3)

10 Write a Verilog code for AND Gate. (3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 (a). Draw the internal circuit of TTL NAND gate circuit and explain.(8 Marks) (14)

(b). Add the following numbers using the 2's complement method.

(i) +38 and -22 (ii) +64 and -29 (iii) +49 and -37 (6 Marks)

12 (a) Express the following decimal numbers into Excess three code, Octal numbers, Grey code forms. (i) 6 (ii) 82 (iii) 524 (9 Marks) (14)

(b) Draw the circuit diagram of a CMOS NOR Gate. Write its truth table. (5 Marks)

Module 2

13 Design a BCD to Decimal Decoder. (14)

14 (a). Implement the following Boolean function using 8:1 MUX. (14)

$F(A,B,C,D) = \prod M(0,1,3,5,7)$(8 Marks)

(b).Realize a full Subtractor using NAND gates only.(6 Marks)

Module 3

15 a). Design a MOD – 12 Asynchronous counter using JK Flip Flop with timing diagram.(9 Marks) (14)

b). Draw the logic diagram of a 4 bit seriel input/ serial output register. Indicate inputs, output and a negative edge triggered clock. (5 Marks)

16 (a). Design a 4 bit asynchronous up counter with timing diagrams.(9 Marks) (14)

(b). Draw the logic diagram of a 4 bit parallel input/ parallel output register. Indicate inputs, output and a negative edge triggered clock. (5 Marks)

Module 4

17 a) Design the circuit of a 4 bit Ring counter. Show the timing Signals also. (5 Marks) (14)

b) With suitable diagram, explain the operation of a DAC. What is meant by Resolution. Determine the resolution of (a). 6 bit DAC (b). 12 bit DAC in terms of percentage. (9 Marks)

18 Design a JK Counter that goes through states 3,4,6,7 and 3.....Is the counter self starting? Modify the circuit such that whenever it goes to an invalid state it comes back to state 3. (14)

Module 5

19 a). Implement Full adder using PLA (10 Marks) (14)

b). Draw the structure of a 32 x 4 ROM using a decoder. (4 Marks)

20 a). Write Verilog Code for a full subtractor circuit.(6 Marks) (14)

b) Differentiate between SRAM and DRAM with diagrams. (8 Marks)

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