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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S,FE) (FT/WP) (S1 PT) Examination May 2025 (2019 Scheme)

Course Code: CST203

Course Name: Logic System Design

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1 Perform the following operations as indicted:

a) $(614)_8 - (10000)_8$ using 8's complement method (1.5)

b) $(614)_8 - (10000)_8$ using 7's complement method (1.5)

2 Perform the following operations as indicated:

a) Find the reflected code equivalent to $(496)_{10}$ (1)

b) Find the r's and (r-1)'s complement of $(18C)_{16}$ (2)

3 Prove that (B+D)(D+C)(A+D) = D+ABC using laws of boolean algebra (3)

4 If F= Σm(1,4,5,7), find the minimized POS using k-map (3)

5 Design a 3 bit parallel adder. Show its working with an example. (3)

6 Realize the function F=Σm(1,3,5,6) using 4x1 MUX (3)

7 Draw the logic circuit of clocked SR flip flop and derive its truth table, characteristic table, characteristic equation and excitation table. (3)

8 Explain triggering of Flip-flops. (3)

9 Represent -6.25 in single precision and double precision IEEE 754 binary floating point format. (3)

10 Implement a minimized PLA of the following multiple output boolean function: (3)

F1(A ,B ,C,D) = Σm(2,4,5,6,7,10,14,15)
F2(A,B ,C,D) = Σm(4,5,9,11,15)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 a) Perform subtraction using r's complement and (r-1)'s complement method

i) $(1001010)_2 - (1010)_2$ (5)

ii) $(321)_4 - (122)_4$ (5)

b) Perform BCD addition of $(2A6)_{16}$ and $(5CF)_{16}$ (4)

12 a) Describe the different schemes for representing negative numbers in binary with examples. (4.5)

b) Perform the operations as indicated:
   i) Convert $(89.625)_{10}$ to equivalent binary, octal and hexadecimal number (4.5)
   ii) Subtract $(8E4B)_{16}$ from $(B74E)_{16}$ using 15's complement and 16's complement method. (5)

Module 2

13 a) Find the minimized SOP and POS for the following functions using k-map: (10)
   i) $F1 = \Sigma m(1,2,5,8,12,13,15) + d(3,9,10)$
   ii) $F2 = \Pi_M(2,8,9,12,14).d(1,4,6,7,11)$
   Here d defines don't care.
   b) Apply DeMorgan's theorem to the following expressions: (4)
   i) (AB' + C'D + EF)'
   ii) (A'B (C + D') + E)'

14 a) Implement the expression using NAND gates only: (6)
   (AB)' (C ((DE)' + (AB)') + BCE)
   b) Convert the given functions into canonical SOP and POS
   i) f(a,b,c) = ac'+ab'c+ab'c' (4)
   ii) f(a,b,c) = (a+c)(a+c')(a'+b+c) (4)

Module 3

15 a) Design and implement a full adder combinational circuit. Also implement the full adder using two half adders. (10)
   b) Draw a logic circuit for magnitude comparison of two 2-bit binary numbers. (4)

16 a) Design and implement a 4-bit odd parity checker, considering the receiver receives the 4-bits as x, y, z and p. Where p is the parity bit generated at sender side. (7)
   b) Design and implement a BCD adder. (7)

Module 4

17 a) Design and implement a 3-bit synchronous UP counter using T flip-flop. Show the logic circuit and timing sequences. (7)
   b) Design and implement a 3-bit asynchronous DOWN counter using T flip-flop. Show the logic circuit and timing sequences. (7)

18 Design and implement an asynchronous decade counter using JK flip-flop. Explain the operations with timing diagram. (14)

Module 5

19 Draw and explain the flow chart for addition and subtraction of binary floating point numbers. (14)

20 a) Implement a 4-bit bidirectional shift register with parallel load. (10)
   b) Find the decimal equivalent of given floating point number expressed in IEEE 754 single precision format: $(11000001111101100000000000000000)_2$ (4)

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