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(Pages 2)

Name.....

Reg. No.....

SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2010

IT 04 604—COMPUTER ARCHITECTURE

(2004 Admissions)

Time : Three Hours

Maximum : 100 Marks

Answer **all** *questions.*

I. (a) Explain the use of registers as internal storage in a processor.

(b) What are the different types of control flow change instructions ? Briefly explain using examples.

(c) What are the advantages of Dynamic scheduling ?

(d) Explain the working of a Branch prediction buffer scheme.

(e) What are the different ways of writing onto cache ? Explain.

(f) What are the primary replacement strategies that are used in cache memory ? Explain.

(g) Explain the various hardware synchronization mechanisms used for multi-processors.

(h) Write the steps involved in transferring a message from one node to another.

(8 × 5 = 40 marks)

II. (a) Describe the characteristics of various classes of Instruction set Architecture. (15 marks)

Or

(b) (i) What are the different ways of encoding an instruction ? Give the format of each scheme and explain.

(10 marks)

(ii) Explain the use of forwarding in Data Hazard. (5 marks)

III. (a) Explain the various methods that are used for preserving. Exception behaviour using Hardware support.

(15 marks)

Or

(b) Explain the working of Two-level predictors. (15 marks)

IV. (a) Discuss the issues related to embedded computer cache design. (15 marks)

Or

(b) (i) Explain the techniques used in the reduction of cache miss penalty. (10 marks)

(ii) Discuss the issues related to unix file system performance. (5 marks)

Turn over

V. (a) Classify switches. Describe the features of each type. (15 marks)

Or

(b) Explain the directory based cache coherence protocol using a state transition diagram. (15 marks)

[4 × 15 = 60 marks]