Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (R,S) / (WP), S4 (PT) Exam April 2025 (2019 Scheme)

Course Code: ECT304

Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1		List advantages of SoC.	(3)
2		Explain the significance of power considerations in VLSI.	(3)
3		Differentiate transmission characteristics of NMOS and PMOS transistors?	(3)
4		Realize XOR gate using CMOS logic.	(3)
5		List the advantages of dynamic logic circuits over static logic circuits.	(3)
6		Explain NP logic.	(3)
7		Mention the worst-case delay associated with Carry-Bypass adder, Linear Carry-Select adder, Square- root carry select adder.	(3)
8		Draw basic block diagram of 16 bit carry bypass adder.	(3)
9		Compare dry and wet oxidation.	(3)
10		Differentiate dry and wet etching process.	(3)

PART B

Answer one full question from each module, each carries 14 marks.

Module I

11	a)	With neat diagram explain the design flow of ASIC.	(10)
	b)	Compare 3 types of Gate array based ASICs.	(4)

OR

12	a)	What is FPGA? Draw and explain internal architecture of FPGA. List out its applications.	(8)
	b)	Describe steps involved in physical design of an integrated circuit.	(6)

Module II

13	a)	Derive expression for the switching threshold of a CMOS inverter.	(8)
	b)	Explain transmission gate logic. Design a 4x1 multiplexer using transmission gate.	(6)

OR

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14 a) Draw and explain voltage transfer characteristics (VTC) of CMOS inverter and describe concept of voltage noise margin in CMOS inverter. (7)

b) Derive expression for total power dissipation in CMOS inverter. (7)

Module III

15 a) Design six transistor SRAM cell and explain read and write operations of SRAM cell. (8)

b) Explain the basic principle of operation in domino logic. (6)

OR

16 a) Illustrate CMOS implementation of a NOR based ROM array to store 4 words of 4 bits each. (7)

b) Draw the circuit diagram of one transistor DRAM cell and explain its read and write operations. Also compare one transistor DRAM with three transistor DRAM. (7)

Module IV

17 a) Design a full adder circuit with CMOS logic using minimum number of transistors. (10)

b) With necessary diagram explain the principle of operation of an array multiplier. (4)

OR

18 a) With block diagram explain a 16-bit linear carry select adder and calculate worst-case delay the circuit. (8)

b) Explain propagate, delete and generate signal. Mention its significance in adder circuits. (6)

Module V

19 a) With necessary diagrams explain production of single crystalline silicon growth by Czochralzki process. (8)

b) Describe iron implantation technique in fabrication process. (6)

OR

20 a) What is photolithography? With diagram illustrate the steps involved in photolithographic process. (8)

b) Explain the role of stick diagram in VLSI design. Draw stick diagram for two input NOR gate. (6)

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