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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech S4 (Minor) Degree Examination May 2025 (2023 Admission)

Course Code: MRT282

Course Name: FUNDAMENTALS OF ANALOG AND DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	Differentiate positive feedback from negative feedback.	(3)
2	Explain the working of Hartley oscillator	(3)
3	Explain Common mode Rejection Ratio of an Operational Amplifier	(3)
4	Draw the circuit diagram of Voltage follower and explain its Application	(3)
5	Compare passive filter and active filter.	(3)
6	Explain Isolation Amplifier	(3)
7	Simplify the expression $Z = AB + A\bar{B}(\overline{\bar{A}\bar{C}})$.	(3)
8	Implement basic gates using universal gates	(3)
9	Explain the working of JK flipflop	(3)
10	Explain a 4 bit PISO Shift Registers	(3)

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Explain the construction, working and characteristics of depletion MOSFET.	(10)
	b)	State Barkhausen criteria. How it is achieved in RC Phase shift Oscillator	(4)
12	a)	Explain the functions of each components in BJT common Emitter amplifier, explain the working and its frequency response Curve.	(10)
	b)	Explain channel pinch off in n channel JFET	(4)

Module -2

13	a)	With the help of a circuit diagram, explain the working of a Non-Inverting Amplifier and derive the expression for closed loop gain.	(9)
	b)	Explain the terms offset voltage and offset current.	(5)
14	a)	Explain the operation of comparator using Op-Amp and explain inverting and non-inverting zero crossing detector.	(9)
	b)	Explain about sample and hold circuits using Op- Amp	(5)

Module -3

15 a) With neat circuit diagram explain the working and frequency response of bandpass filter using Op Amp. (7)

b) Explain different components in PLL. (7)

16 a) Explain the working of monostable multivibrator using 555 timer IC (7)

b) Explain different ranges of operations in PLL with suitable diagrams (7)

Module -4

17 a) Minimize the expression Y=$A\bar{B}C + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}\bar{C}+\bar{A}\bar{B}\bar{C}$ using kmap. (7)

b) Design and implement a full subtractor using basic gates (7)

18 a) Reduce the following function using Karnaugh map technique. F (W, X, Y, Z) = m (0, 7, 8, 9, 10, 12) + d (2, 5, 13). (7)

b) Design and implement a gray to binary converter (7)

Module -5

19 a) Design 3 bit synchronous up counter using T Flip flops. (14)

20 b) Design a 3it up down asynchronous counter using Jk flip flop (14)

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