Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (R,S) Exam April 2025 (2019 Scheme)

Course Code: ECT312

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

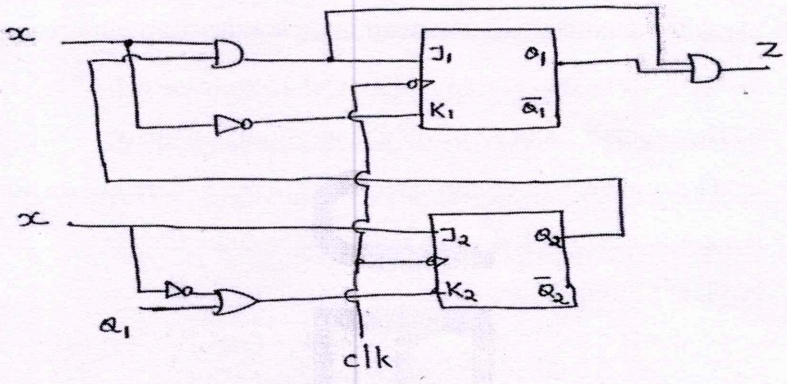
1	List the main components of ASM chart.	(3)
2	Differentiate between Mealy and Moore models.	(3)
3	What are cycles and races in asynchronous sequential circuits?	(3)
4	What is input restricted flow table in Asynchronous Sequential networks?	(3)
5	Explain jitter? List the sources of clock jitter.	(3)
6	Define Hazards. Mention types of hazards	(3)
7	Define Stuck at 0 fault and Stuck at1 fault.	(3)
8	Define fault detection, fault isolation and fault diagnosis.	(3)
9	What are FPGA? What are the advantages of FPGA?	(3)
10	Differentiate between CPLD and FPGA.	(3)

PART B

Answer one full question from each module, each carries 14 marks.

Module I

11 a) Analyze the following clocked synchronous sequential network. Construct the excitation table, transition table, state table and state diagram (8)



b) Draw the ASM chart for a Mod-6 counter (6)

OR

12 a) Using implication chart construct the minimal state table from the state table given below. (8)

Present state	Next state		output	
	Input(x)		Input(x)	
	0	1	0	1
A	A	B	0	0
B	D	C	0	1
C	F	E	0	0
D	D	F	0	0
E	B	G	0	0
F	G	C	0	1
G	A	F	0	0

b) Obtain the state diagram and state table for the clocked synchronous sequential network having a single input line x in which the symbols 0 and 1 are applied and a single output line z. An output of 1 is to be produced if and only if the three input symbols following two consecutive input 0's consist of at least one 1. At all other times the output is to be 0. An example of input/output sequences that satisfy the conditions of the network specifications is (6)

x = 0100010010010010000000011

y = 0000001000000100000000001

Module II

13 a) Obtain a primitive flow table and a minimal row flow table for a fundamental mode asynchronous sequential network meeting the following requirements. (9)

a. There are two inputs x1 and x2 and a single output z.

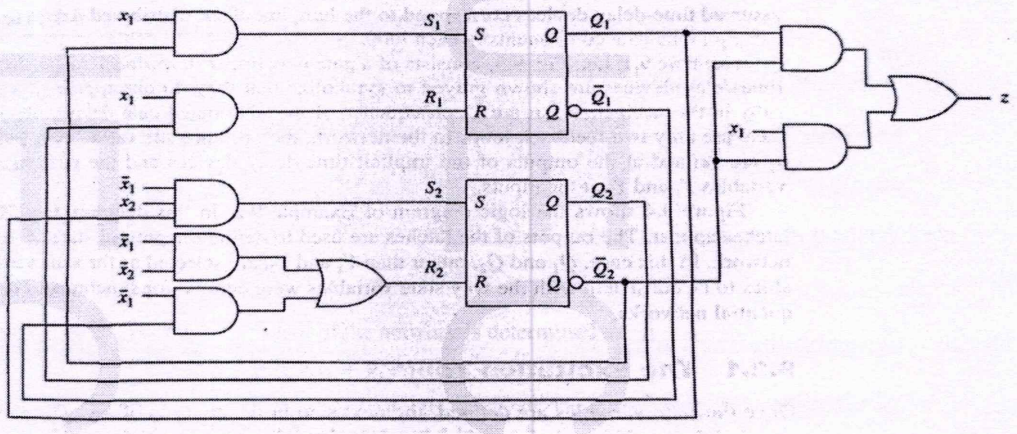
b. The inputs x1 and x2 never change simultaneously.

c. The output is to be the same as x1 if x2 = 1. However, if x2 =0, the output is to remain fixed at its last value before x2 became 0.

b) Explain primitive flow table. (5)

OR

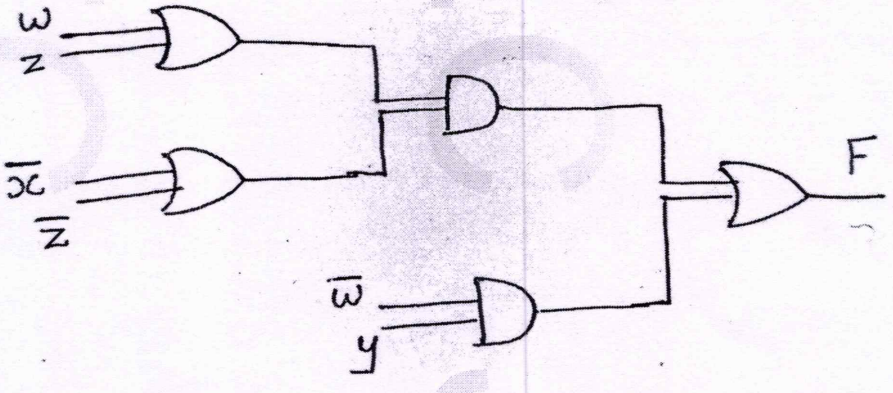
14 a) Analyze the asynchronous sequential network by forming the excitation table, transition table, state table, flow table and flow diagram. The network operates in fundamental mode with the restriction that only one input variable can change at a time. (9)



b) Draw and explain the general structure of an asynchronous sequential network with time delay devices. (5)

Module III

15 a) Determine all the Static 1 and Static 0 hazard. Re-design the network to be hazard free. (8)



b) How can the timing problems in asynchronous sequential circuits be solved using mixed operating mode circuits? (6)

OR

16 a) Examine the possibility of hazard in the AND-OR logic circuit whose Boolean function is given by $f = \sum m(3,4,6,7)$. Show how the hazard can be detected and eliminated. (7)

b) Describe the concept of switch bouncing and suggest a suitable solution. (7)

Module IV

17 a) A circuit realizes the function $f = x_1x_2x_3 + x_1x_2x_4 + x_3'x_4$. Using Boolean difference method, find the test vectors for SA0 faults and SA1 faults on the input line x_3 of the circuit. (8)

b) Write note on BIST techniques. (6)

OR

18 a) Describe the fault table method used for effective test set generation for the circuit whose logic equation is $y = x_1x_2+(x_2+x_3)'$ (8)

b) Explain the principle of path sensitisation method (6)

Module V

19 a) Explain the architecture of XC4000 FPGA family. (7)

b) Explain switch matrix in Xilinx XC9500 CPLD. (7)

OR

20 a) With suitable diagram explain the architecture of XC9500. (7)

b) With suitable diagram explain the input – output block architecture of FPGA XC4000 (7)

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