Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R,S) (FT/WP) / (S2 PT) Examination April 2025 (2019 Scheme)

Course Code: EET206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	Express the decimal number -26 as an 8-bit binary number in sign magnitude form, 1's complement form and 2's complement form	3
2	Convert $(100110)_2$ to BCD , Excess -3 and gray code.	3
3	With neat logic diagram, explain how OR gate can be represented using NAND gates alone.	3
4	With a neat figure, explain how basic 2-bit parallel adder is implemented using two full-adders.	3
5	Explain with neat diagram, the working of 4:1 multiplexer.	3
6	Explain how exclusive-NOR gate can be used in basic single bit comparator.	3
7	Draw the circuit of 4-bit Ring counter along with the output table.	3
8	Determine the number of flip-flops needed to design (i) a mod-2 counter (ii) a decade counter (iii) a 3 bit register.	3
9	Explain the advantage of the R-2R ladder DAC over the weighted resistor type DAC.	3
10	Give the Verilog code for (i) OR gate (ii) Half Adder	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	What is mean by parity? Explain how the error detection is done using even and odd parity scheme with examples.	(7)
	b)	Explain the concept of noise margin with reference to logic families. Is it better to have a lower value of noise margin or a higher value? Which logic family (CMOS or TTL) is preferable in high noise environment and why?	(7)
12	a)	Subtract 39 from 83 using 8 bit 1's complement and 2's complement methods. Compare both the methods.	(8)
	b)	Explain the following performance parameters of logic families. (i) Fanout (ii) Propagation Delay (iii) Power dissipation	(6)

Module -2

13	a)	The Boolean Expression for exclusive-OR gate is $\bar{A}B + A\bar{B}$. Using this as starting point, apply De Morgan's theorems and any other Boolean laws to develop an expression for exclusive NOR gate.	(6)
	b)	Reduce the expression using K map in SOP form. Y=f (A,B,C,D) =$\sum$m(6,7,8,10,11,15) + d(0,2,3,4,5,9,14)	(8)
14	a)	Explain with neat diagram how a full adder can be implemented using half adders.	(6)
	b)	Obtain the simplified POS expression using K map. Y=f (A,B,C,D)=$\sum$ m(1,3,7,11,15) + d(0,2,4)	(8)

Module -3

15		Explain 7 segment LED display. With relevant logic diagram, truth table and K map simplification, explain the design of BCD to seven segment decoder. Draw the detailed logic circuit diagram of the decoder.	(14)

16	a)	Design a 4-bit binary to gray code converter.	(10)
	b)	Implement the function f=∑m (1,3,5,6) using 8 to 1 mux.	(4)

Module -4

17	a)	Draw the circuit diagram and timing diagram for a 3 bit ripple up counter using negative edge triggered D Flip flop. Explain.	(4)
	b)	Design a mod 6 synchronous up counter using JK flip flops.	(10)
18	a)	Explain the procedure to convert D Flip-Flop to SR Flip-Flop with neat circuit diagram.	(6)
	b)	Design an asynchronous decade counter using T flipflop.	(8)

Module -5

19	a)	Distinguish between Moore and Mealy machines.	(4)
	b)	With neat diagrams and taking an example, explain the working of Successive Approximation type ADC.	(10)
20	a)	With neat diagram, explain flash type ADC.	(8)
	b)	Differentiate between PAL and PLA. Illustrate the implementation of SOP expressions using both.	(6)

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