Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (S, FE) Examination December 2024 (2019 Scheme)

Course Code: ECT312

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

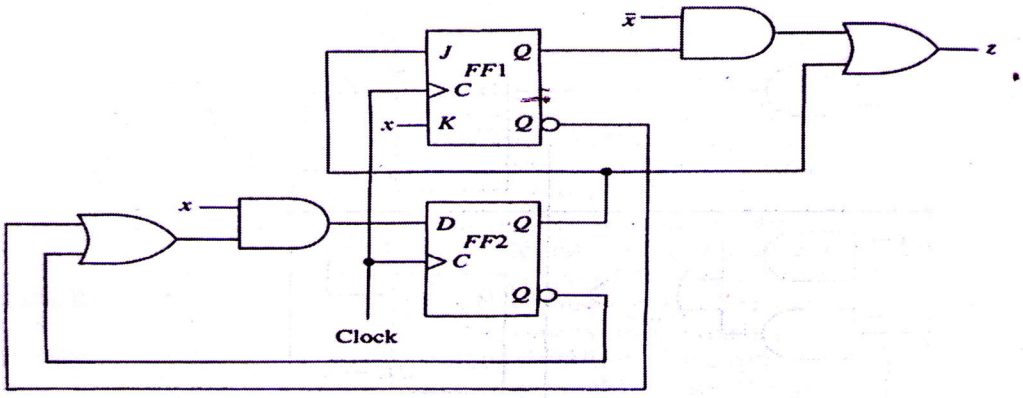
1	Distinguish synchronous and asynchronous sequential logic circuits.	(3)
2	Explain state table with an example.	(3)
3	When does race conditions arise in an asynchronous sequential circuit?	(3)
4	What are the steps for the reduction of input restricted flow table?	(3)
5	Explain static1 and static 0 hazard.	(3)
6	List different types of clock jitter.	(3)
7	Define Stuck at 0 fault and Stuck at1 fault.	(3)
8	Define test vector, test set and test generation.	(3)
9	Explain the three major components of a FPGA architecture.	(3)
10	What are FPGA? What are the advantages of FPGA?	(3)

PART B

Answer one full question from each module, each carries 14 marks.

Module I

11 a) Analyze the following clocked synchronous sequential network. Construct the excitation table, transition table, state table and state diagram (9)



b) Draw the ASM chart for a Mod-5 counter (5)

OR

12 a) Design a serial Binary adder as a Mealy network using D flipflop (8)

b) Obtain the state diagram and state table for the clocked synchronous sequential network having a single input line x in which the symbols 0 and 1 are applied and a single output line z. An output of 1 is to be produced if and only if the three input symbols following two consecutive input 0's consist of at least one 1. At all other times the output is to be 0. An example of input/output sequences that satisfy the conditions of the network specifications is (6)

x = 0100010010010010000000011

y = 0000001000000100000000001

Module II

13 a) Obtain a primitive flow table and a minimal row flow table for a fundamental mode asynchronous sequential network meeting the following requirements. (9)

a. There are two inputs x1 and x2 and a single output z.

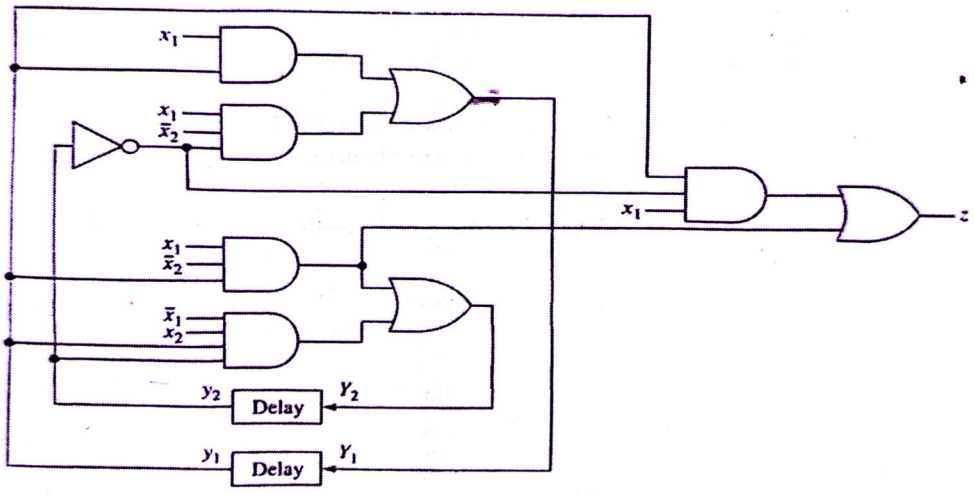
b. The inputs x1 and x2 never change simultaneously.

c. The output is to be 1only when the values of x1 and x2 are both the same and x2 was the variable that changed value causing x1 and x2 to become the same.

b) Draw and explain the general structure of an asynchronous sequential network with time delay devices. (5)

OR

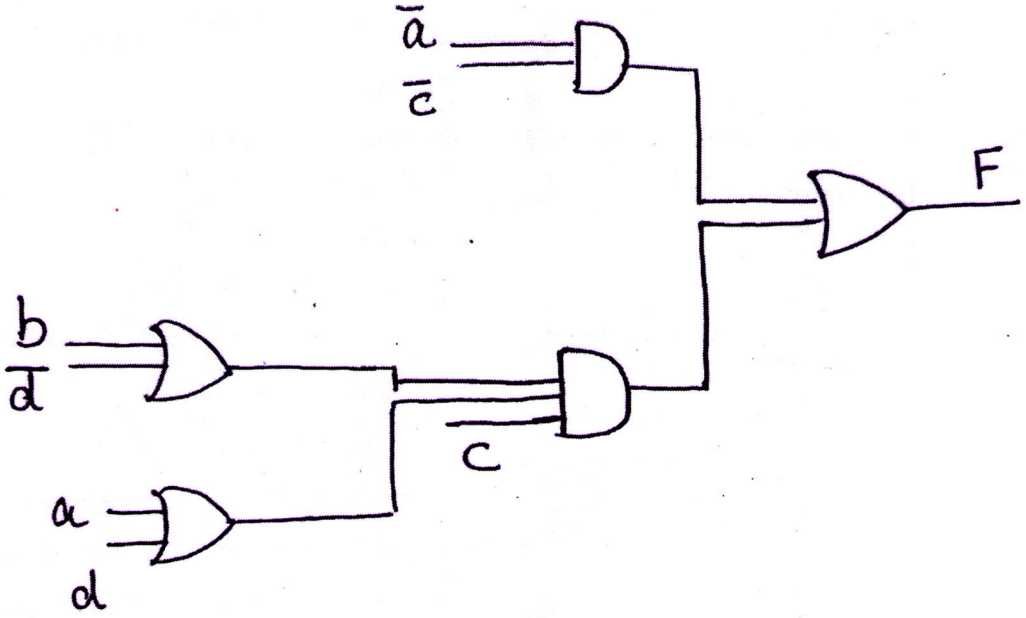
14 a) Analyze the asynchronous sequential network by forming the excitation table, transition table, state table, flow table and flow diagram. The network operates in fundamental mode with the restriction that only one input variable can change at a time. (9)



b) Explain merger diagram with an example. (5)

Module III

15 a) Find all the static hazard in the given network. For each hazard, specify the values of the variable which are constant and the variable which are changing. Indicate how all these hazards could be eliminated by adding gates to the existing network. **(9)**



b) Explain dynamic hazards. **(5)**

OR

16 a) Examine the possibility of hazard in the OR-AND logic circuit whose Boolean function is given by f = ∑m (0,2,4,5). Show how the hazard can be detected and eliminated. **(9)**

b) What do you mean by clock skew? Differentiate between positive skew and negative skew. **(5)**

Module IV

17 a) A circuit realizes the function $f = x_1x_2 + x_3x_4$. Using Boolean difference method, find the test vectors for SA0 fault on the input line x_1 of the circuit. (8)

b) Explain path sensitisation method with example. (6)

OR

18 a) Find the test vectors of all sa0 and sa1 faults of the circuit whose Boolean function is $f = x_1x_3 + x_1x_4 + x_2x_3 + x_2x_4$ by the Kohavi algorithm. (8)

b) Write note on BIST techniques (6)

Module V

19 a) Draw the simplified block diagram of Xilinx XC4000 configurable logic block and explain the various sections. (7)

b) With suitable diagram explain the input – output block architecture of CPLD XC9500 (7)

OR

20 a) Explain the architecture of XC4000 FPGA family with the help of block diagram. (7)

b) Explain switch matrix in Xilinx XC9500 CPLD. (7)

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