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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S, FE) / S2 (PT) (S, FE) / S4 (WP) (S) Examination December 2024 (2019 Scheme)

Course Code: EET 206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1 Subtract 32 from 21 using 8-bit 2's complement arithmetic. Write the necessary steps. (3)

2 Compare the performance of TTL and CMOS logic families. (3)

3 Express the Boolean function, $f(X,Y,Z) = XY + \bar{X}Z$ as product of maxterms. (3)

4 Derive an expression for the sum of a full adder. (3)

5 Implement the sum of minterms expression, $f(A,B,C) = \sum m(0,1,5,6)$ using a 4:1 multiplexer. (3)

6 List three functions of Arithmetic and Logic Unit (ALU). (3)

7 Derive the characteristic equation of a J-K flip-flop. (3)

8 What is meant by *'race around'* in flip-flops? How it can be eliminated? (3)

9 Draw the circuit diagram of a 4-bit weighted resistor type digital to analog converter (DAC). Write an expression for its output. (3)

10 Define any three performance parameters of an analog to digital converter (ADC). (3)

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11 a) Perform the following number conversions: (6)

(i) $(476.37)_8$ to binary.
(ii) $(A9C.FB)_{16}$ to octal.
(iii) $(101110.101)_2$ to decimal.

b) Explain CMOS NOR gate with the help of internal diagram. (8)

12 a) Find out equivalent decimal number if 1101101 is expressed in (i) sign-magnitude form (ii) 1's complement form (iii) 2's complement form. (6)

b) With the help of a neat internal diagram, explain the working of TTL NAND gate. (8)

Module -2

13 a) With the help of a truth table, derive an expression for the difference and borrow bits of a full subtractor. Draw the logic diagram. (8)

b) Simplify the Boolean function $f(A,B,C,D) = \sum m(1,4,5,6,7,10,12) + d(8,11,13)$ (6)

14 a) Simplify the Boolean functions to minimum number of literals: (6)

(i) $f(P,Q,R,S) = P + Q[PR + (Q + \bar{R})S]$

(ii) $f(X,Y,Z) = \overline{(X + \overline{YZ})}\,(X\bar{Y} + XYZ)$

b) With a neat circuit diagram explain the working of a 4-bit parallel adder. What is its drawback when compared to a carry look-ahead adder? (8)

Module -3

15 a) Write down the truth table of a 2 to 4 decoder with active-low enable input and active-high outputs. Implement this decoder using AND and NOT gates. (5)

b) Design and implement a 4-bit binary to Gray code converter. (9)

16 Write down the truth table for a BCD-to-seven segment decoder. Deduce the Boolean expression for each output. (14)

Module -4

17 a) Convert an S-R flip-flop to a J-K flip flop. Write the necessary truth table. (6)

b) What is a shift register? Draw the logic diagram of a 4-bit serial-in, serial-out (SISO) shift register using D flip-flops. Explain its operation with the help of an example. (8)

18 a) Draw the logic circuit diagram of a 4-bit ring counter which employs D flip-flop. Write down its count sequence table. (5)

b) Design a mod-10 asynchronous up-counter using J-K flip-flops. Draw the timing diagram and relevant excitation table. (9)

Module -5

19 a) What is PAL? List three advantages of PAL over PLA. (5)

b) Draw the block diagram of a successive approximation type ADC. Explain how it converts an analog signal to a digital signal. (9)

20 a) List any four applications of FPGA. (4)

b) Implement a full adder in Verilog. Draw the necessary logic circuit and truth table. (10)

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