B

0200CST202122401

Pages: 2

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S, FE) / S2 (PT) (S, FE) / S4 (WP) (S) Examination December 2024 (2019 Scheme)

Course Code: CST 202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		Explain the steps involved in the execution of an instruction.	3
2		Write the control sequence for the execution of conditional branch instruction.	3
3		Draw and explain about true/complement circuit?	3
4		Describe about logic and shift micro operations. Listing the available operations in each category.	3
5		Explain the steps involved in restoring division.	3
6		Describe about instruction pipeline.	3
7		Differentiate between horizontal and vertical microinstructions.	3
8		Explain PLA based control organization with the help of a diagram.	3
9		What are interrupts? List the sequence of steps following an interrupt request?	3
10		Draw and explain the memory hierarchy.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Describe the following addressing modes with suitable examples. i) Relative addressing mode ii) Register addressing mode iii)Auto increment addressing mode iv) Immediate addressing mode	8
	b)	Differentiate between big endian and little endian byte ordering with examples	6
12	a)	Write the three-address, two-address and one-address representations of the given operation (A+B) * (C+D) with relevant assumptions.	6
	b)	Explain multi-bus organization with neat sketches. Write the control sequence for the instruction Add R4, R5, R6 for the multi-bus organization.	8

Module -2

13	a)	Explain 4 bit complete accumulator with neat sketches.	8

	b)	Describe processor organization with diagram using i) scratchpad memory ii) Two-port memory	6
14	a)	Illustrate and explain the organization of a processor unit where processor registers and ALU are connected through common buses. Explain how the micro operation R1 ← R2+R3 would be performed using this organization, where R1, R2 and R3 are processor registers.	7
	b)	Design a 4-bit combinational logic shifter with two control variables, H1 and H0. Specify the operations for each control variable and explain its working.	7

Module -3

15	a)	Draw the flowchart of Booth's multiplication algorithm and multiply -9 X -13	10
	b)	Design and draw the block diagram for a 3 by 2 array multiplier.	4
16	a)	List and explain the different pipeline hazards and their possible solutions.	10
	b)	Write notes on arithmetic pipeline.	4

Module -4

17	a)	Design a hardwired control unit used to perform addition/subtraction of numbers represented in sign magnitude form.	14
18	a)	With the help of a diagram explain the functioning of a micro-program sequencer in a micro-programmed controlled processor?	10
	b)	Write a note on Sequence register and decoder method.	4

Module -5

19	a)	Explain in detail about the mechanisms for accessing I/O devices?	8
	b)	List and explain the different types of ROMs.	6
20	a)	Explain the various mapping functions available in cache memory.	9
	b)	Briefly explain content addressable memory.	5

***