Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (S, FE) / S4 (PT) (S, FE) Examination December 2024 (2019 Scheme)

Course Code: ECT304

Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

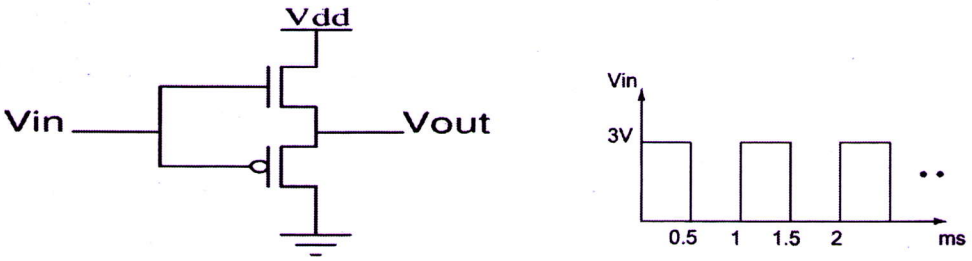
Answer all questions, each carries 3 marks Marks

1 What is ASIC? Draw the block diagram showing its various classifications. (3)

2 Comment on the performance features of FPGA based design. (3)

3 Draw the DC characteristics of CMOS inverter and mark the regions of operation of NMOS and PMOS transistors as input is varied from 0 to V_{dd}. (3)

4 Show the output waveform, Vout for the following input pattern. Given V_{dd} =3V, V_{tn}=|V_{tp}|=1V. Assume zero rise and fall delay. (3)



5 Implement AB+CD in domino logic. (3)

6 Compare DRAM and SRAM cells. (3)

7 Express sum and carry output of a full adder in terms of propagate and generate signal. (3)

8 Give the value for critical path delay for 16 bit carry bypass adder and 4* 4 array multiplier. Assume $t_{sum} = t_{mux} = t_{carry}$ = 10ns and $t_{setup} = t_{and}$ =5ns. (3)

9 Comment on Wet and Dry oxidation. (3)

10 Draw the stick diagram of two input CMOS NAND gate. (3)

PART B

Answer one full question from each module, each carries 14 marks.

Module I

11 a) Explain in detail ASIC Design flow. (8)

b) Differentiate between Channelled and channel less gate array. (6)

OR

12 a) With neat diagram explain the structure of an FPGA. (9)

b) Comment on Top down and Bottom Up design methodologies. (5)

Module II

13 a) Comment and compare two NMOS inverters with enhancement type and depletion type NMOS load operated in saturation region. (6)

b) Implement two input XOR and XNOR in static CMOS logic and pass transistor logic. (8)

OR

14 a) Derive the expression for V_{IH} & V_{IL} for a static CMOS inverter. (10)

b) Comparison between switch implemented using transmission logic and pass transistor logic. (4)

Module III

15 a) Draw and explain NORA logic. How will you connect NORA logic to a NMOS domino logic ? (7)

b) Comment the working of 3 transistors (3-T) DRAM. (7)

OR

16 a) Comment on charge sharing issue in domino logic. Explain any method to reduce it. (8)

b) Implement a 4 * 4 NOR based ROM to store the following data 1100,1010, 1001 and 0110. (6)

Module IV

17 a) Explain the mechanism of carry bypassing in improving critical path delay in adder design. (4)

b) With neat implementation diagram explain the working of 4*4 array multiplier. (10)

OR

18 a) Explain with diagram working of an N bit square root carry select adder. (8)

b) Implement transistor structure of sum and carry of a full adder in static CMOS structure. (6)

Module V

19 a) Describe in detail the manufacturing steps of single crystal Silicon from Quartzite(sand). (10)

b) Describe the λ rule to be followed in connecting wires. (4)

OR

20 a) With neat diagram explain molecular beam epitaxy. (8)

b) Draw the circuit diagram and layout of static CMOS inverter. (6)

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