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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S, FE) Examination June 2024 (2019 Scheme)

Course Code: MRT203

Course Name: ANALOG AND DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1		Explain Barkhausen criteria.	(3)
2		Explain the concept of pinch-off in JFET.	(3)
3		What are the characteristics of an ideal op-amp?	(3)
4		Discuss the concept of offset current and offset voltage in op-amp.	(3)
5		Analyse the frequency response of a band stop filter.	(3)
6		Implement a frequency multiplier using PLL.	(3)
7		Simplify the Boolean expression Y = $\bar{Q}R + P\bar{Q}\bar{R} + PQR + \bar{P}QR$.	(3)
8		Implement half adder using logic gates.	(3)
9		Differentiate synchronous counters and asynchronous counters.	(3)
10		Analyse the factors influencing the Race-Around condition in JK flip-flop and formulate a design approach to solve this issue.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11	a)	Explain Hartley Oscillator with the help of a circuit diagram.	(7)
	b)	Explain the operation of a Class B power amplifier.	(7)
12	a)	With diagram explain the working of common emitter amplifier	(7)
	b)	Discuss the construction of a JFET and analyse its characteristics.	(7)

Module 2

13	a)	Obtain the expression for output voltage of a differentiator. Support your answer with necessary circuit diagram.	(7)
	b)	Design a non-inverting amplifier with gain 8.	(7)
14	a)	Evaluate the output of an op-amp comparator. Support your answer with necessary circuit diagram and waveforms.	(8)
	b)	Evaluate the output of a sample and hold circuit.	(6)

Module 3

15	a)	Draw and explain the pin diagram of 555 IC timer	(7)
	b)	Explain the working of 555 IC timer as an astable multivibrator with neat diagram	(7)
16	a)	Analyse first order low pass filter with help of a circuit diagram and frequency response plot.	(9)
	b)	Explain the working of PLL with a neat diagram.	(5)

Module 4

17	a)	Design a full subtractor using logic gates.	(9)
	b)	Design a Multiplexer using logic gates	(5)
18		Simplify the given expression using Quine McCluskey method $F(a,b,c,d)=\sum m\ (0,1,2,5,6,7,8,9,10,14)$	(14)

Module 5

19		Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 1010 is detected.	(14)
20	a)	Discuss about a serial in serial out shift register. Analyse with an example.	(7)
	b)	Design a modulo 3 counter using flip flops.	(7)