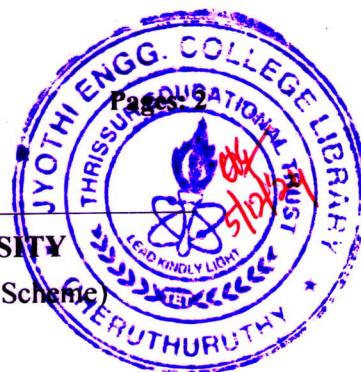


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Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (R,S) Examination November 2024 (2019 Scheme)

Course Code: RAT205

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks

Marks

- | | | |
|----|--|-----|
| 1 | Convert the hexadecimal number $(2C)_{16}$ into binary and octal | (3) |
| 2 | Write a short note on ASCII code | (3) |
| 3 | Implement NOT gate and AND gate using NAND gate only | (3) |
| 4 | Explain De Morgans theorem | (3) |
| 5 | List the application of shift register | (3) |
| 6 | Differentiate between asynchronous and synchronous counter | (3) |
| 7 | Explain the term accuracy and resolution for D/A converter | (3) |
| 8 | Draw the basic connection diagram for DAC-08 | (3) |
| 9 | Compare flash SSD memory and SRAM | (3) |
| 10 | Design an AND gate using verilog code | (3) |

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

- | | | | |
|----|---|--|-----|
| 11 | a | Add the following numbers using the 2's complement method.
(i) +18 and -27 (ii) +54 and -19 | (7) |
| | b | Explain the working of a typical CMOS NAND gate with necessary diagram | (7) |
| 12 | a | Which are the basic gates? Explain the working of each basic gates using truth table? | (7) |
| | b | Convert the decimal number $(82.025)_{10}$ to binary, hexadecimal and Excess-3 Code? | (7) |

Module 2

- 13 a Explain the working of three bit Carry Look ahead adder with the help of diagram? (7)
- b Simplify the Boolean expression $F(A,B,C,D) = \sum m(1, 3, 5, 7, 8, 9, 11, 13, 15)$ using K map? (7)
- 14 a Explain the working of an decoder that decodes BCD to decimal digits with necessary equations, table and diagram? (7)
- b Explain the working of full subtractor with truth table and circuit diagram? (7)

Module 3

- 15 a Explain the working of a D Flip flop with necessary diagrams, state and excitation table? (7)
- b Convert a JK Flip flop into a SR Flip flop (7)
- 16 a Design a 4 bit asynchronous down counter with circuit and timing diagram (7)
- b Draw the timing and circuit diagram of SISO 4-bit register for the data input 1010. The register initially contains all 1s. (7)

Module 4

- 17 a Explain the working of a 6-bit Ring Counter with circuit and timing Diagram (7)
- b Explain the working of R-2R ladder type D to A converter. (7)
- 18 a Design a 4 bit synchronous binary up counter with circuit and timing Diagram? (7)
- b Explain the working of successive approximation type A/D converter (7)

Module 5

- 19 a Explain the working of PROMs and EPROMs. (7)
- b Write the Verilog code for a half adder. (7)
- 20 a Explain the architecture of FPGA. (7)
- b Write the Verilog code for $S = \sum m(1, 2, 5, 7)$ (7)
