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Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
 B.Tech Degree S3 (R,S) Examination November 2024 (2019 Scheme)



Course Code: MRT203

Course Name: ANALOG AND DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions. Each question carries 3 marks*

- | | | Marks |
|----|---|-------|
| 1 | Discuss about the concept of feedback. | (3) |
| 2 | Evaluate the criteria used to obtain sustained oscillations. | (3) |
| 3 | With a circuit diagram briefly explain an isolation amplifier. | (3) |
| 4 | List the characteristics of an ideal op-amp. | (3) |
| 5 | Discuss any one application of PLL. | (3) |
| 6 | Analyse the frequency response of a band pass filter. | (3) |
| 7 | Briefly discuss about NAND, XOR, OR logic gates. | (3) |
| 8 | Simplify the Boolean expression $Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + \bar{A}\bar{B}\bar{C}$. | (3) |
| 9 | Explain in detail about master-slave JK flip-flop. | (3) |
| 10 | Discuss about SR flip flop. | (3) |

PART B*Answer any one full question from each module. Each question carries 14 marks***Module 1**

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|----|----|--|-----|
| 11 | a) | Discuss the operation of Colpitts Oscillator with the help of a circuit diagram. | (7) |
| | b) | Explain RC phase shift oscillator with a neat circuit diagram. | (7) |
| 12 | a) | Explain the construction of a depletion type MOSFET | (7) |
| | b) | Explain the characteristics of JFET | (7) |

Module 2

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|----|----|--|-----|
| 13 | a) | Design an inverting amplifier with gain 6. | (7) |
| | b) | Obtain the expression for gain of a non-inverting amplifier. | (7) |
| 14 | a) | Obtain the expression for output voltage of an integrator. Support your answer with necessary circuit diagram. | (8) |
| | b) | Evaluate the operation of a voltage to current converter with circuit diagram and necessary equations. | (6) |

Module 3

- 15 Evaluate the operation of 555 timer as a monostable multivibrator. Draw necessary circuit diagram and waveforms. (14)
- 16 a) Analyse first order high pass filter with help of a circuit diagram and frequency response plot. (9)
- b) Explain the working of VCO with a neat diagram. (5)

Module 4

- 17 a) Design a full adder using logic gates. (8)
- b) Design a 1 to 8 De-Multiplexer using logic gates. (6)
- 18 Design a 4-Bit binary to Gray code converter. (14)

Module 5

- 19 a) Design a 3-bit synchronous up counter using D flips flop. (8)
- b) Design a mod 5 asynchronous counter. (6)
- 20 Design a sequence detector that produces output 1 whenever a sequence 1001 is detected. (14)
