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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (R,S) / S3 (WP) (R,S) / S1 (PT) (S,FE) Examination November 2024 (2019 Scheme)

Course Code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 **Duration: 3 Hours**

PART A

Answer all questions. Each question carries 3 marks Marks

1 In a number system with base r, $(13)_r + (30)_r = (103)_r$. Determine the base/radix r. (3)

2 Write down the table for 3-bit Gray code and mention its advantages over other binary codes. (3)

3 Show that an XOR gate is associative. (3)

4 Determine the complement (F') of function $F(a,b,c) = a\bar{b} + bc$ and show that $F + F' = 1$. (3)

5 Explain the gate level modelling in Verilog with the aid of a suitable example. (3)

6 Implement a 4-input binary encoder with truth table. (3)

7 Explain race around condition in flip flops. (3)

8 Describe the steps in converting a JK flip flop into D flip flop. (3)

9 Define noise margin of a logic gate and explain its significance. (3)

10 Define the terms fan-in and fan-out with respect to a logic gate. (3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 a) Perform the following operations using 2's complement arithmetic. (8)

(i) 111010 - 01101

(ii) 29.625 – 56.5

b) Explain the various operators in Verilog. (6)

12 a) Perform the following arithmetic operations. (8)

(i) Hexadecimal addition: $(B9)_{16} + (F3)_{16}$.

(ii) BCD addition : 686 + 237

b) Explain fixed and floating point representation of numbers. (6)

Module 2

13 (a) Determine the minimal SOP expression for the given function $F(a,b,c,d) = \sum m(0,2,4,6,7,8,10,11,12) + d(3,14)$ using Karnaugh maps. (8)

(b) Implement the function obtained in question (a) above using basic logic gates and using NAND gates alone. (6)

14 (a) Determine the minterms and maxterms in the canonical form of $F(w,x,y,z) = x(\bar{y} + z) + wy$. (8)

(b) Write a Verilog code for implementing the above function. (6)

Module 3

15 (a) Implement the function $F(A,B,C) = AB + B\bar{C} + \bar{A}\bar{B}C$ using (10)

(i) 8:1 MUX (ii) 4:1 MUX

(b) Realize the function given above using 3:8 decoder. (4)

16 (a) Design a 3-bit comparator circuit and draw the circuit diagram. (7)

(b) Write the Verilog code for 1:8 demultiplexer. (7)

Module 4

17 Design a synchronous counter using T flip flops that counts through the following sequence 0-2-3-7-9-11-15-0-... The counter should be reset in case any unused state is reached. (14)

18 (a) Explain the working of JK flip flops with the help of excitation table and characteristic equations. (6)

(b) Draw the circuit diagram of 4-bit SIPO shift register and explain the working with the aid of timing diagrams. (8)

Module 5

19 (a) Compare TTL, CMOS and ECL logic families in terms of noise margin, propagation delay and power dissipation. (6)

(b) Draw the circuit diagram of TTL 2-input NAND gate and explain its working. (8)

20 (a) Draw the circuit diagram of CMOS 2 input NOR gate and explain the working with the help of truth table. (7)

(b) Explain ECL gate with the help of an example circuit. (7)

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