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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (R,S) / S3 (WP) (R,S) / S1 (PT) (S,FE) Examination November 2024 (2019 Scheme)

Course Code: CST203

Course Name: Logic System Design

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1 Represent +100 and -100 in signed magnitude, 1's complement and 2's complement form. (3)

2 Find corresponding Binary, Octal and Hexadecimal numbers. $(646.875)_{10}$. (3)

3 Draw the circuit for the expression X+YZ by using,
   a) NOR gate only
   b) NAND gate only.

4 Define and prove Demorgan's law. (3)

5 Design magnitude comparator. (3)

6 Design gray to binary code convertor. (3)

7 What is meant by triggering? What are the types of triggering? (3)

8 Differentiate synchronous and asynchronous circuits. (3)

9 Give the IEEE single precision and Double precision floating point representations. (3)

10 Differentiate Ring and Johnson counters. (3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 a) Perform the following operations. (6)

$(456)_8 + (123)_8$

$(456)_8 - (173)_8$

$(5B69)_{16} + (7AC3)_{16}$

$(1ADB)_{16} - (1A70)_{16}$

b) Describe ASCII and EBCIDIC coding scheme. (4)

c) Add and Subtract the BCD numbers 1000 and 0101. (4)

12 a) Find Binary, 1's complement, 2's complement, BCD, excess-3, 9's complement and 10's complement of the decimal number $(1028)_{10}$. (7)

b) Explain weighted and non weighted codes with examples. (3)

c) What you meant by self reflecting Binary code? Explain with example. (4)

Module 2

13 a) Design a combinational circuit with 3 inputs and one output. The output of circuit is 1 when the decimal value of the inputs is greater than 2. (7)

b) Explain Boolean algebra laws. (7)

14 a) Convert F = A + B'C into standard SOP form and POS form. (7)

b) Solve the following using K-map and verify by Quine Mccluskey method. $f(A,B,C)=\sum(0,1)+d(2,4,6)$ (7)

Module 3

15 a) Design a 4x2 encoder circuit. (7)

b) Design even parity code generator. (7)

16 a) Design full adder and full subtractor and represent by using both universal gates. (14)

Module 4

17 a) Design SR flip flop, JK flipflop, T flipflop and D flipflop. Explain with suitable diagrams, tables and equations. (14)

18 a) Design 4 bit asynchronous up counter. (7)

b) Design a 4 bit synchronous down counter. (7)

Module 5

19 a) Illustrate the algorithms for, (14)

1. Signed magnitude addition.
2. Floating point addition.
3. BCD Addition.

20 a) Explain the different types of shift registers. (7)

b) Describe PLA with suitable example. (7)

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