Reg No.:_____ Name:_____

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

Eighth Semester B.Tech Degree Supplementary Examination August 2024 (2019 Scheme)

**Course Code: CST464**

**Course Name: EMBEDDED SYSTEMS**

**Max. Marks: 100** **Duration: 3 Hours**

**PART A**

***Answer all questions, each carries 3 marks.*** **Marks**

| | | | |
|---|---|---|---|
| 1 | | Explain the role of a watchdog timer in an embedded system. | (3) |
| 2 | | Explain about the characteristics of an embedded System. | (3) |
| 3 | | What is the difference between Data Flow Graph (DFG) and Control Data Flow Graph (CDFG) | (3) |
| 4 | | Define Hardware- Software Co-design. List out the advantages of Hardware Software co-design. | (3) |
| 5 | | Explain about any two task synchronization issues. | (3) |
| 6 | | What is the difference between 'Hard' and 'Soft' real-time systems? Give an example for 'Hard' and 'Soft' real-time systems. | (3) |
| 7 | | List out the advantages and limitations of the super-loop based approach over an RTOS based approach. | (3) |
| 8 | | What are the three main objectives of Embedded product Development Life Cycle? | (3) |
| 9 | | Explain the need for a timewheel in IoT. | (3) |
| 10 | | Discuss about Beacon transmission. | (3) |

**PART B**

***Answer any one full question from each module, each carries 14 marks.***

**Module I**

| | | | |
|---|---|---|---|
| 11 | a) | Discuss about the Embedded System Design Process with suitable diagrams. | (8) |
| | b) | Illustrate the Embedded System Design Process using GPS moving map module as an example. | (6) |

**OR**

| | | | |
|---|---|---|---|
| 12 | a) | Describe any four on-board communication interfaces used in embedded systems. | (14) |

**Module II**

| | | | |
|---|---|---|---|
| 13 | a) | Draw an FSM model for coin operated telephone system. | (10) |
| | b) | Discuss about the issues in hardware software co-design. | (4) |

**OR**

14 a) Design and Draw a concurrent processing model for the Seat Belt Warning System of an automobile. Clearly specify your assumptions in the design. (10)

b) Define Hardware software trade-off. List out the hardware software trade off components. (4)

**Module III**

15 a) Discuss about the functional requirement to be considered while selecting RTOS for Embedded System. (8)

b) Explain about Priority inversion and solutions for priority inversions. (6)

**OR**

16 a) Consider the set of 5 processes whose arrival time and burst time are given below- If the CPU scheduling policy is SJF preemptive, calculate the average waiting time and average turnaround time. (8)

| Process Id | Arrival time | Burst time |
|---|---|---|
| P1 | 3 | 1 |
| P2 | 1 | 4 |
| P3 | 4 | 2 |
| P4 | 0 | 6 |
| P5 | 2 | 3 |

b) Explain how mutual exclusion through busy waiting and semaphore is implemented for task synchronisation. (6)

**Module IV**

17 a) Explain the need for EDLC. Illustrate with a neat diagram the different phases of an EDLC life cycle. (14)

**OR**

18 a) Illustrate any 5 different approaches used for embedding firmware into the hardware of an embedded device. (14)

**Module V**

19 a) Illustrate the working of a battery-operated smart card reader with suitable diagram (10)

b) Draw the UML sequence diagram of IoT smart appliance device with explanation. (4)

**OR**

20 a) Differentiate between Flexray and LIN network along with its pros and cons. List out any three applications of these networks. (14)

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