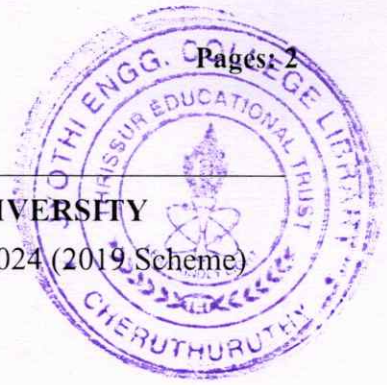


Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S, FE) Examination June 2024 (2019 Scheme)

**Course Code: RAT205****Course Name: DIGITAL ELECTRONICS**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions. Each question carries 3 marks*

Marks

- | | | |
|----|--|-----|
| 1 | Convert the decimal number $(928)_{10}$ to excess-3 code | (3) |
| 2 | Convert the hexadecimal number $(EF)_{16}$ into binary and decimal | (3) |
| 3 | Explain De morgan's theorem | (3) |
| 4 | Explain about SOP and POS forms | (3) |
| 5 | Convert J K flip flop to T flip flop | (3) |
| 6 | Explain the working of serial in serial out shift register | (3) |
| 7 | Explain the working of weighted resistor type D to A converter | (3) |
| 8 | Explain the terms gain error and offset error | (3) |
| 9 | What are the main characteristics of flash SSD memory? | (3) |
| 10 | Design an OR gate using verilog code | (3) |

PART B*Answer any one full question from each module. Each question carries 14 marks***Module 1**

- | | | | |
|----|---|--|-----|
| 11 | a | Perform the addition of signed numbers -57 and +28 using 1's complement method and 2's complement method | (7) |
| | b | Write notes on (i) power dissipation (ii) fan out (iii) fan in (iv) noise margin | (7) |
| 12 | a | Which are the universal gates. Explain the working of XOR and XNOR gates using truth table | (7) |
| | b | Convert the decimal number $(53.125)_{10}$ to binary, hexadecimal and octal number system | (7) |

Module 2

- 13 a Simplify the Boolean expression $F(A,B,C,D) = \sum m(1, 3, 5, 7, 8, 9, 11, 13,15)$ (7)
using K map
- b Explain the working of full adder with truth table and circuit diagram . (7)
- 14 a Implement the following Boolean function using 8:1 MUX. (7)
 $F(A, B,C,D) = \sum m (1,4,5,8,12,15)$
- b Explain the working of 4-bit ripple carry adder (7)

Module 3

- 15 a Explain the working of a SR Flip flop with necessary diagrams, state and (7)
excitation table
- b Convert a SR Flip flop into a JK Flip flop (7)
- 16 a Design a mod 11 asynchronous up counter with circuit and timing diagram (7)
- b Draw the timing and circuit diagram of SIPO 4-bit register for the data input (7)
0110. The register initially contains all 1s .

Module 4

- 17 a Explain the working of a 5-bit Johnson Counter with circuit and timing (7)
Diagram
- b Draw the basic connection diagram for DAC-0808 and familiarize the (7)
components
- 18 a Design a 4-bit synchronous binary up counter using T Flip flop with circuit and (7)
timing diagram
- b Explain the working of flash type A to D converter (7)

Module 5

- 19 a Explain the working of static RAM and dynamic RAM (7)
- b Write the Verilog code for a full adder (7)
- 20 a Implementing a Sum-of-Products Expression using PAL (7)
 $S = \sum m (1,2,5,9,10)$
- b Write the Verilog code for $S = \sum m (1,2,5,7)$ (7)
