Reg No.:_____ Name:_____

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth Semester B.Tech Degree (R,S) Examination May 2024 (2019 Scheme)

Course Code: ECT312

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each question carries 3 marks. Marks

1	Differentiate between Mealy and Moore models.	(3)
2	List out the steps in state table reduction using implication chart method.	(3)
3	What is fundamental mode in asynchronous sequential circuits?	(3)
4	In asynchronous sequential circuits, how does a state table differ from a flow table?	(3)
5	Define clock skew. Explain the different types.	(3)
6	Differentiate between synchronous and asynchronous inputs of a sequential circuit.	(3)
7	List the different types of faults in digital circuits.	(3)
8	Distinguish between essential, selective and redundant test vectors in fault detection.	(3)
9	Differentiate between CPLD and FPGA.	(3)
10	What is configurable logic block in FPGA?	(3)

PART B

Answer one full question from each module, each question carries 14 marks.

Module I

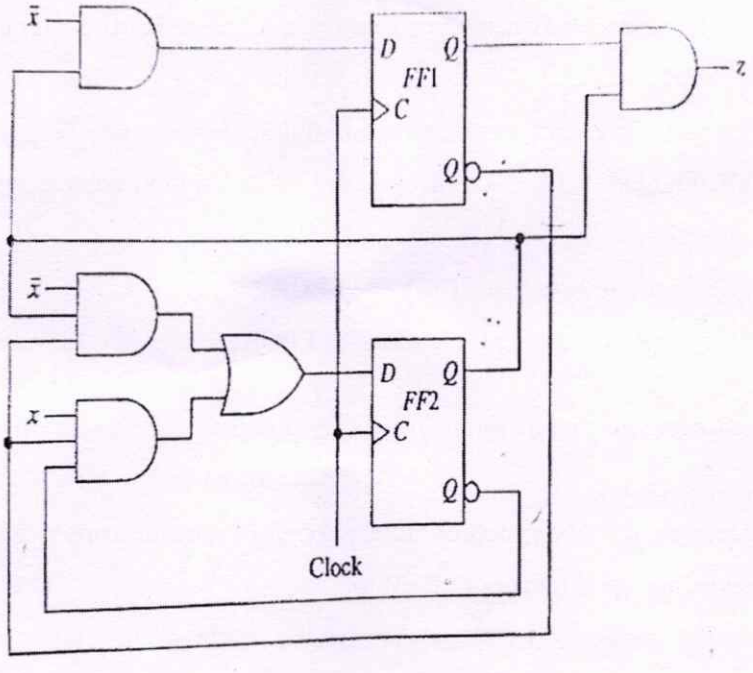
11	a)	Design a clocked synchronous sequential Moore network to detect the overlapping sequence of 110 using D flipflop.	(7)
	b)	Using implication chart, construct the minimal state table from the state table given below.	(7)

Present state	Next state		output	
	Input(x)		Input(x)	
	0	1	0	1
A	B	C	0	0
B	C	D	1	0
C	B	E	0	0
D	F	E	0	0
E	G	A	0	0
F	F	H	1	0
G	A	D	1	0
H	D	F	1	1

OR

12 a) Draw the ASM chart for a Serial Binary Adder as Mealy Network. (6)

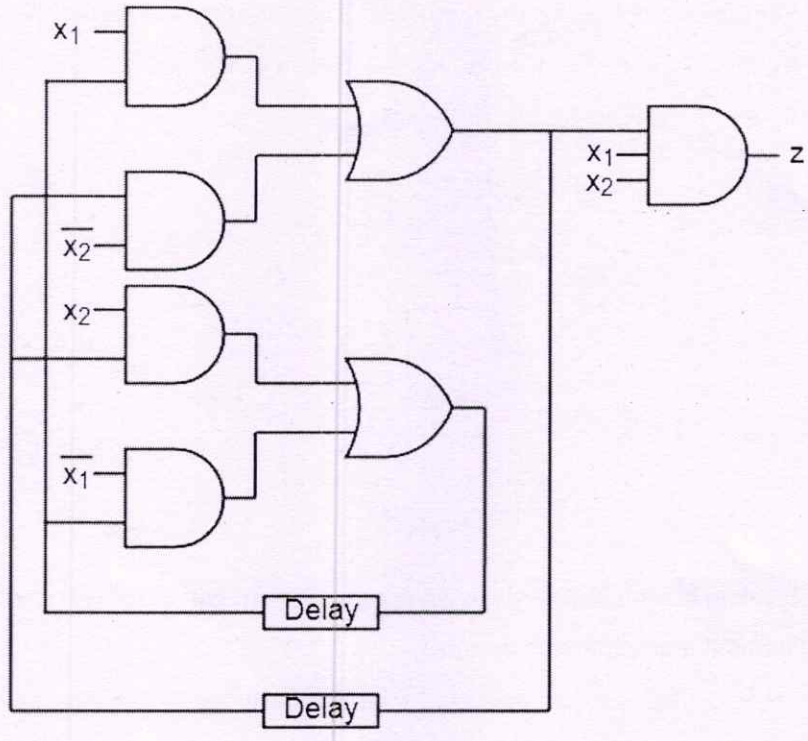
b) Analyse the following clocked synchronous sequential network. Construct the excitation table, transition table, state table and state diagram. (8)



Module II

13 a) Explain races in asynchronous sequential circuits with the aid of a suitable example. (6)

b) Examine the Asynchronous Sequential Circuit shown below to generate the excitation/transition table, state table, flow table and flow diagram. (8)



OR

14 Define a primitive flow table. Establish a primitive flow table for designing an Asynchronous Sequential Circuit which meets the following requirements: (14)

(i) There are 2 inputs x1 and x2 and single output z.

(ii) The inputs x1 and x2 never change simultaneously.

(iii) The output is always to be 0, when x1 =0, independent of the value of x2.

(iv) The output is to become 1 if x2 changes while x1=1 and is to remain 1 until x1 becomes 0 again.

Also obtain the reduced flow table by applying the flow table reduction techniques.

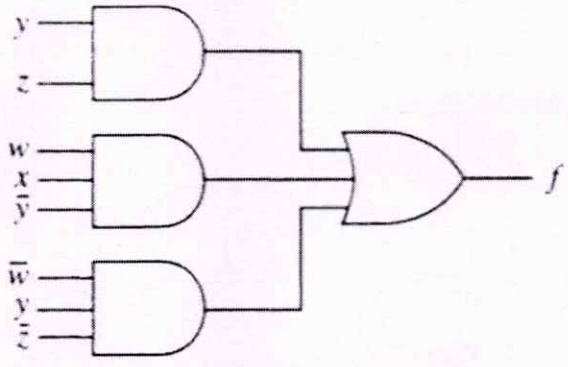
Module III

15 a) Explain the problem of contact bounce in switches and show how an SR latch can eliminate the problem by suitable illustrations. (7)

b) With a suitable circuit and waveforms, explain the functioning of a Data Synchronizer. (7)

OR

16 a) For the gate network shown in figure, determine all the static 1 & static 0 hazards. Redesign the network to be hazard free and having the same output gate as in figure. (8)



b) Explain essential hazards in asynchronous sequential networks and how it can be avoided in a sequential circuit. (6)

Module IV

17 a) A circuit realizes the function $z=x_1'x_4+x_2'x_3+x_1x_4'$. Using the Boolean difference method, find the test vectors for SA0 faults and SA1 faults on the input line x_1 of the circuit. (8)

b) Write a note on Automatic Test Pattern Generation. (6)

OR

18 a) Illustrate the fault table method used for effective test set generation for the circuit whose Boolean function is z = x1'x2+x3 and find the minimal test set. Identify the redundant test vector. (8)

b) Write a note on BIST techniques. (6)

Module V

19 a) With a suitable diagram, describe the input-output block architecture of Xilinx 9500 CPLD family. (7)

b) Explain the architecture of XC 4000 FPGA family. (7)

OR

20 a) Explain switch matrix in Xilinx XC9500 CPLD. (7)

b) Using suitable illustrations explain the XC4000 programmable interconnect. (7)

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