Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S,FE) / S3 (PT) (S,FE) Examination June 2024 (2015 Scheme)

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Convert the decimal numbers 456.50 and 164.75 to binary, octal and hexadecimal. (6)

b) What is meant by the Hamming code? A noisy channel is used to send the message "1101101," which is coded in the 7-bit even parity Hamming code. Decode the message, assuming that at most a single error occurred in each code word (6)

c) Perform the following conversions (3)

i) 25_{10} *to BCD*

ii) 152_{10} *to Excess* 3

iii) 1101011001 *to gray code*

2 a) Using K-map, obtain the minimal sum of the product of the following expression and realize using NAND gates only. (8)

$$F(ABCD) = \sum m(0,2,3,5,7,12,15) + \sum d(1,6,14)$$

b) Consider two numbers $A = A_1A_0$ and $B = B_1B_0$. Design a combinational circuit to compare these numbers and generate outputs Z_1 *if* $A = B$, Z_2 *if* $A < B$ *and* Z_3 *if* $A > B$ (7)

3 a) Design a full adder using 3-to-8-line decoder and gates (6)

b) Design and realise using 8 X 1 multiplexer (3)

$$f(A,B,C,D) = \sum m(0,2,3,6,7)$$

c) Perform the following operations (6)

i) $DCEA_{16} + 4BF1_{16}$

ii) $734_8 - 526_8$

iii)$110101)_2 - 1010)_2$ using 1's and 2's complement method

PART B

Answer any two full questions, each carries 15 marks.

4 a) Sketch the two input TTL NAND gate in totem pole configuration and with the help of truth table explain its operation. (7)

b) Using NAND gates implement the JK flip-flop and explain the operation with truth table, excitation table and characteristic equation. (8)

5 a) Define the terms noise margin, voltage and current levels and power dissipation of logic families. Prepare a table that compares the above values of the TTL, ECL, and CMOS logic families. (7)

b) Design a MOD 5 asynchronous counter using JK flip-flop. (8)

6 a) Compare PAL and PLA with the help of example. (5)

b) Design a 3-bit synchronous up-counter using T flipflop (10)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Draw the logic diagram of a 4-bit Ring counter and explain the working with truth table and timing diagram. (10)

b) Design the logic circuit using JK flip-flop for the given state table where X is the input. Draw the state diagram, transition table, D flip-flop excitation table, logic diagrams. (10)

Present state	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
A	A	C	0	0
B	A	C	1	0
C	A	D	0	0
D	A	D	0	1

8 a) Design a 2-bit synchronous up/down counter using T flipflop that counts up when the control signal M=1 and counts down when M=0. (10)

b) Design a circuit to detect the sequence 110 with overlapping, using D FF. Draw the state diagram, state table, excitation table and the logic circuit. (10)

9 a) Explain the working of a 4-bit SISO and 4-bit PIPO register with the help of logic diagram and timing diagram. (10)

b) Reduce the following state table using equivalence class state reduction technique. (10)

Present state	Next state and output			
	X=0		X=1	
A	A	0	B	0
B	E	0	C	0
C	H	0	B	0
D	C	1	G	0
E	G	0	F	0
F	F	1	E	1
G	B	1	G	0
H	D	0	I	0
I	I	1	H	1

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