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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R,S) / S4 (WP) (R) / S2 (PT) (S, FE) Examination May 2024 (2019 Scheme)

Course Code: CST 202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1	Explain how the PC, IR, MAR and MDR registers are used during the instruction execution cycle.	3
2	What information is conveyed by the addressing mode used in an instruction? List any four addressing modes.	3
3	Explain shift microoperation with help of examples.	3
4	Illustrate the processor organisation using scratchpad memory with help of a diagram.	3
5	Illustrate divide overflow condition in restoring division with help of an example.	3
6	Differentiate between unifunction and multifunction pipelines.	3
7	Draw the block diagram for a control unit using PLA based organization.	3
8	What is the role of next address generator in microprogrammed control organization?	3
9	Does Direct Memory Access increase the efficiency of processor? Justify your answer.	3
10	Explain the need for using cache memory within the computer system.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	What do you mean by byte addressable memory? Explain the two different types of byte assignment using diagrams.	7
	b)	Illustrate processor organisation using a single bus with help of a diagram. Explain how register transfers and ALU operations are carried out in the single bus organisation.	7

12 a) Describe the following addressing modes, giving an example for each: 7

i) Indirect Addressing mode

ii) Immediate Addressing mode

iii) Indexed Addressing mode

b) Discuss how instructions are classified based on number of operands or addresses they use. 7

Module -2

13 a) What is the role of status register within the processor? Draw the circuit diagram for a basic status register for an 8-bit ALU and explain how the carry and overflow status bits are set. 7

b) What is a control word? Explain, using an example, how a control word can be used to specify a complete instruction. 7

14 a) Draw the circuit diagram and function table for one stage of the logic unit for a 4-bit ALU with following logic operations – AND, OR, XOR and NOT. Explain the working. 7

b) Illustrate the use of accumulator register. Explain processor organization using accumulator register with help of a diagram. 7

Module -3

15 a) Explain the advantage of using an array multiplier. Design a 3x2 array multiplier. 7

b) Briefly describe the following with reference to pipelining: 7

i) Clock period

ii) Speedup

iii) Efficiency

iv) Throughput

16 a) Illustrate Booth's Multiplication algorithm with help of a flowchart and an example. 7

b) Summarize the different techniques used for pipeline hazard resolution. 7

Module -4

17 a) Are there any advantages in using PLA based or microprogrammed control organizations when compared to the hardwired organizations? Explain your answer. 7

b) Illustrate, with a diagram, how a microprogram sequencer helps to generate next address in a microprogrammed control organization. 7

18		Summarize, with help of an example, the steps involved in designing a hardwired control organization using one flip flop per state method.	14

Module -5

19	a)	Explain the basic structure of a DRAM cell. Why does DRAMs need constant refreshing?	7
	b)	How does the processor react when an interrupt is raised by an I/O device?	7
20	a)	What is a ROM? List and explain the different types of ROMs.	7
	b)	What are two modes in which Direct Memory Transfer can operate? Explain their differences.	7

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