Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S6 (S, FE) / S4 (PT) (S,FE) Examination May 2024 (2015 Scheme)

Course Code: EC304

Course Name: VLSI

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) Explain the techniques used for growing single crystal Silicon from polycrystalline silicon. (8)

b) Apply Deal Grove model to find the thickness of the oxide deposited after a time 't' of oxidation. (7)

2 a) Explain the various stopping mechanisms during ion implantation. What is the dominant ion stopping mechanism for a) heavy ions b) high energy ions? Discuss the reason. (8)

b) With necessary steps, explain the process of transferring a pattern from a mask to a wafer with positive photo resist. (7)

3 a) With a neat diagram explain the Molecular Beam Epitaxy technique. (6)

b) With neat diagrams, discuss the steps involved in the fabrication of bipolar junction transistors. (9)

PART B

Answer any two full questions, each carries 15 marks

4 a) Explain the operation of CMOS inverters with its voltage transfer characteristics. Find the switching threshold and also V_{IH}. (9)

b) Determine t_{pHL} and t_{pLH} of CMOS inverters. Find the values of W/L ratio of PMOS to make the $t_{pHL}=t_{pLH}$ (6)

5 a) Draw a) circuit diagram b) stick diagram c) layout of 2 input NAND gate. (10)

b) Implement $Y = \overline{A + B(C + DE)}$ using static CMOS logic. (5)

6 a) Implement an XOR gate using pass transistor logic. What is the limitation of the circuit? How can it be eliminated using transmission gate logic? Also implement XOR function using transmission gate logic. (10)

b) Find the logical effort of a 3 input NAND gate having the same propagation delay as that of a simple CMOS inverter. (5)

PART C

Answer any two full questions, each carries 20 marks

7 a) Explain how read and write operations are performed in a 3 Transistor DRAM cell. (10)

b) Explain the working of a differential voltage sensing amplifier, How does it improve the working of a SRAM cell? (10)

8 a) Explain working principle of a 20 bit adder built using 4 bit carry bypass adder blocks. Find the worst case propagation delay of the circuit (10)

b) Design a MOS 4x4 NAND ROM to store 1100,0110,0111,0011. Explain its working. (10)

9 a) With a circuit, explain the working of a mirror adder. Discuss its features which make it a good alternative to conventional static CMOS inverter. (10)

b) Explain the working of 4X4 array multiplier. Mark the worst case propagation delay paths in the block diagram. (10)

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