Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S7 (S, FE) / S5 (PT) (S, FE) Examination May/June 2024 (2015 Scheme)

Course Code: CS405

Course Name: Computer System Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

		Marks
1	State Amdahl's law. Suppose that we want to enhance the processor used for a server machine. The new processor is 15 time faster on computation in the serving applications than the original processor. Assuming the original processor is busy with computation 30% and waiting for I/O 70% time, what is the overall speedup gained by incorporating the enhancement	(4)
2	Explain UMA model for multiprocessor system.	(4)
3	Define inclusion property of memory hierarchy.	(4)
4	Discuss the role of process migration and i/o in cache inconsistency.	(4)
5	Differentiate worm hole routing and store and forward routing.	(4)
6	Explain chained cache coherence protocol.	(4)
7	Define data hazard. What are the three types of data hazards?	(4)
8	What do you mean by pipeline stalling? Explain with an example	(4)
9	Discuss the principle of multithreading.	(4)
10	Elucidate the context switching policies.	(4)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	State Bernstein's conditions for checking parallelism among a set of processes.	(3)
	b)	Analyse the data dependence of the following statements and construct a dependency graph. Also detect the parallelism embedded in it S1: LOAD R1,M(100) S2:MOVE R2,R1 S3:INC R1 S4:ADD R2,R1 S5:STORE m(100),R1	(6)
12	a)	Discuss about UMA and NUMA model.	(6)
	b)	Explain memory hierarchy.	(3)

13 a) Explain Flynn's classification of computer architecture. (6)

b) Describe the property of locality of reference in memory. (3)

PART C

Answer any two full questions, each carries 9 marks.

14 a) With a neat diagram discuss about generalized multiprocessor system. (3)

b) Describe the components of hierarchical bus system. (4)

c) With examples differentiate between single stage and multistage network. (2)

15 a) Write notes on message routing schemes. (3)

b) Explain different flow control strategies. (6)

16 a) Discuss the structure of multiport memory with a neat diagram. (3)

b) Describe a crossbar network. Explain about the design of a crosspoint switch with a neat diagram. (6)

PART D

Answer any two full questions, each carries 12 marks.

17 a) What is Instruction pipelining? Explain in detail. (4)

b) Discuss about prefetch buffers. (4)

c) Discuss about inorder and out of order issue processor. (4)

18 a) Describe about the two types of latency problem. (6)

b) Explain the structure and working of a pipeline processor with multiple functional units. (6)

19 a) Outline the latency hiding mechanisms. (6)

b) Describe the two solutions for asynchrony problem. (6)

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