D

02000EET206052104

Pages: 2

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (S, FE) / S2 (PT) (S) Examination January 2024 (2019 Scheme)

Course Code: EET206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	Implement NOT circuit using a two input EX-OR gate.	3
2	Subtract decimal number 22 from 17 using 8 bit 2's complement method.	3
3	Using the Boolean laws and rules, simplify the logic expression $Z = (\bar{A} + B)(A+B)$	3
4	Convert the following function into standard POS and express as maxterms $Y(A,B,C)=(A+B)\ (B+\bar{C})\ (A+C)$	3
5	Draw the circuit for a 4 x 1 MUX and explain operation.	3
6	Draw the circuit for Decimal to BCD encoder circuit and explain.	3
7	Determine the number of flip-flops needed to construct a register capable of storing (i) a 6 bit binary number (ii) hexadecimal numbers upto F (iii) octal numbers upto 10.	3
8	Draw the circuit and timing diagram for a 2 bit ripple counter using D Flip flop.	3
9	Draw the circuit of flash ADC and explain.	3
10	Write the structural mode of three input AND gate in Verilog HDL.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Convert the following i) $(1001011)_{gray} = (\ )_2$ ii) $(10110110.0011)_2 = (\ )_{BCD}$ iii) $(5762)_8 = (\ )_{16}$ iv) $(76)_{10} = (\ )_{gray}$ v)Attach the proper even parity bit to 10100100 and odd parity bit to 11111000.	10
	b)	Convert the decimal number 3.248×10^4 to a single-precision floating-point binary number.	4
12	a)	With example explain any two representations for signed binary numbers	4
	b)	Explain the working of TTL NAND gate with the help of internal diagram.	10

Module -2

13	a)	Using k-map determine the minimal sum of product expression and realize the simplified expression using only NAND gates $f(w, x, y, z) = \pi M(0, 2, 3, 7, 8, 9, 10)$	10
	b)	Show that a full adder can be constructed with two half adders and an OR gate.	4
14	a)	Use a K-map to simplify $AC[\bar{B} + B(B + \bar{C})]$ to a minimum SOP form.	4
	b)	Realise a 4 bit look ahead carry adder. What is the advantage over a ripple adder?	10

Module -3

15	a)	Implement the Boolean function F(A,B,C,D) =Σm(1,3,4,11,12,13,14,15) using 8:1 multiplexer.	7
	b)	Design and draw implementation circuit for an odd parity generator circuit for 4 bit binary data.	7
16	a)	Design two bit comparator using decoder.	8
	b)	Draw the implementation circuit of a 1 : 8 Demultiplexer using two 1 : 4 demultiplexers	6

Module -4

17	a)	Illustrate the conversion of (a) a J-K flipflop into a D flip-flop and (b) a J-K flip-flop into a T flip-flop. Explain.	4
	b)	Show how an asynchronous counter with J-K flip-flops can be implemented having a modulus of twelve with a straight binary sequence from 0000 through 1011. Also draw the timing diagram.	10
18	a)	Design a counter to produce the following binary sequence. Use J-K flip-flops. 1, 4, 3, 5, 7, 6, 2, 1, …	10
	b)	Draw the circuit and timing diagrams of a 3 bit SISO shift register	4

Module -5

19	a)	Explain the working of successive approximation ADC with the help of an example.	10
	b)	Differentiate Moore and Mealy state machines.	4
20	a)	Explain the working of R-2R ladder type DAC with the help of an example. What is its advantage over weighted resistor type DAC?	10
	b)	Compare PAL and PLA with their logic implementation.	4

***