Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree (S, FE) Examination January 2024 (2015 Scheme)

Course Code: EC212

Course Name: LINEAR INTEGRATED CIRCUITS AND DIGITAL ELECTRONICS (MC)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks. Marks

1 List out the characteristics of an ideal op-amp. (5)

2 Describe positive and negative clippers with circuit diagrams and waveforms. (5)

3 An 8 bit D to A converter has a resolution of 10mV per bit.Find the analog output voltage for the inputs a)10001010 b) 00010000 (5)

4 Convert (5)

(i) $(1011011011)_2$ to hexadecimal

(ii) $(11011.101)_2$ to decimal

(iii) $(5497)_{10}$ to octal

(iv) $(A0F9.0EB)_{16}$ to decimal

(v) $(214)_{10}$ to base 5

5 Draw the truth table of a half subtractor and implement it using logic gates. (5)

6 Compare a static RAM with a dynamic RAM. (5)

7 Specify the excitation table and characteristic equation of RS flip flop. (5)

8 Explain race round condition.How can it be eliminated? (5)

PART B

Answer any three full questions, each carries 10 marks.

9 a) Derive an expression for output voltage of an ideal op-amp integrator. Mention its limitations. Explain a practical integrator with neat diagram. (10)

10 a) Elucidate the working of Schmitt trigger with circuit diagram, waveform and hysteresis loop. (10)

11 a) Explain the working of successive approximation ADC with neat diagram. (10)

12 a) Using a K-map, convert the following standard POS expression (10)

(A'+B'+C+D)(A+B'+C+D)(A+B+C+D')(A+B+C'+D')(A'+B+C+D')(A+B+C'+D)

(i) into a minimum POS expression.

(ii) into a minimum SOP expression.

13 Discuss the need of instrumentation amplifier with diagram. Mention its advantages. (10)

PART C

Answer any two full questions, each carries 15 marks.

14 a) Design and implement a 3 bit binary to Gray Converter. (10)

15 a) Use a multiplexer having 3 input data select to implement the logic for the given function $F=\sum m(0,1,2,3,4,10,11,14,15)$. (10)

16 a) Describe a Parallel in Serial Out (PISO) shift register with a logic diagram. (10)

17 a) Design and implement a 3 bit synchronous down counter. (10)

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