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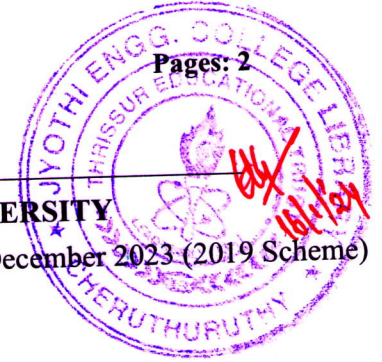
Pages: 2

Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Regular and Supplementary Examination December 2023 (2019 Scheme)



Course Code: RAT 205

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer all questions. Each question carries 3 marks*

Marks

- 1 Convert the gray number 10110010 into (i) hex (ii) octal (iii) decimal (3)
- 2 What are Excess-3 codes? Find the excess-3 code for the decimal number 597. (3)
- 3 Prove  $AB+A'C+BC = AB+A'C$  (3)
- 4 Express the function  $f(A,B,C) = AB + BC$  in standard POS form. (3)
- 5 If MOD-3, MOD-4 and MOD-5 counters are cascaded with input frequency of 18 MHz, what is the number of states and output frequency respectively? (3)
- 6 Draw the truth table of JK flip flop and explain race round condition in JK flip flop. (3)
- 7 Differentiate between synchronous and asynchronous counters. (3)
- 8 Draw and explain 3 bit Johnson counter. (3)
- 9 List three advantages and applications of FPGA. (3)
- 10 Differentiate RAM and ROM. (3)

**PART B**

*Answer any one full question from each module. Each question carries 14 marks*

**Module 1**

- 11 a Perform subtraction using 2's complement method: (8)  
(i)  $(-64)_{10}$  from  $(+32)_{10}$  (ii)  $(29.A)_{16}$  from  $(4F.B)_{16}$ . Use 8 bit representation.  
b Realise basic gates using universal gates. (6)
- 12 a Convert (i)  $(2020.65625)_{10}$  to octal (ii)  $(54673)_8$  to binary (4)  
(iii)  $(1024)_8$  to hexadecimal (iv)  $(1010)_2$  to Gray  
b Explain the working of CMOS NAND gate with the help of internal circuit diagram. (10)

**Module 2**

- 13 a Implement the function  $F(A,B,C) = \sum m(0,2,3,7)$  using 4x1 MUX. (6)

**0800RAT205122101**

- b Reduce the function  $f(A,B,C,D) = A'B'D + ABC'D' + A'BD + ABCD'$  using K map and implement using NAND gates. (8)
- 14 a What is the difference between a parallel adder and a carry look-ahead adder? Explain the operation of carry look-ahead adder. (8)
- b Implement full adder using 3:8 decoder. (6)

**Module 3**

- 15 a Design a MOD-5 asynchronous down counter using T flip flop and explain its operation. Show the timing diagram. (7)
- b Convert JK flip flop to D flip flop. (7)
- 16 a Design a 3 bit asynchronous updown counter using JK flip flop. Show the timing diagram for up and down counting. (10)
- b Explain the working of a parallel in parallel out shift register using the logic circuit. (4)

**Module 4**

- 17 a Draw and explain the working of R-2R ladder Digital to Analog Converter. (10)
- b Explain the working of a 4 bit Johnson counter. (4)
- 18 Design a 4 bit binary synchronous counter using D flip flop. (14)

**Module 5**

- 19 a Write the Verilog code for 8x1 MUX. (6)
- b Differentiate PROM and EPROM. (8)
- 20 a Explain the difference between PLA and PAL devices with the help of internal logic diagrams. (10)
- b Write the Verilog code for half adder. (4)

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