

C

0800MRT203122102

Pages: 2

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Regular and Supplementary Examination December 2023 (2019 Scheme)



Course Code: MRT203

Course Name: ANALOG AND DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks

- | | Marks |
|--|-------|
| 1 Differentiate between BJT and FET. | (3) |
| 2 "Positive feedback is used in oscillators". Justify your answer. | (3) |
| 3 List the characteristics of ideal op amp. | (3) |
| 4 Explain schmitt trigger with neat circuit diagram. | (3) |
| 5 Discuss on active low pass filter. | (3) |
| 6 Explain about Voltage Controlled oscillator. | (3) |
| 7 State and prove De-Morgan's theorem. | (3) |
| 8 Simplify the Boolean expression $Y = \sum m(8,9,10,11,12,14)$ | (3) |
| 9 Compare combinational and sequential circuits. | (3) |
| 10 What is race around condition? How it is eliminated? | (3) |

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

- | | | |
|----|---|------|
| 11 | a) Explain the construction and principle of E-MOSFET with necessary diagrams. | (10) |
| | b) Comment on Barkhausen criteria. | (4) |
| 12 | Explain RC Phase shift oscillator and derive the expression for frequency of oscillation. | (14) |

Module 2

- | | | |
|----|--|-----|
| 13 | a) Draw the functional block diagram of OP AMP and explain each block. | (8) |
| | b) Sketch the basic circuit using OP AMP to perform the mathematical operation of differentiation and explain. | (6) |

- 14 Illustrate the following (14)
- a) V-I converter
 - b) I-V converter
 - c) Isolation amplifier

Module 3

- 15 a) Explain Astable multivibrator using IC 555. (8)
- b) Explain in detail about any one application of PLL (6)
- 16 a) Write a note Band Stop Filter with neat diagram (6)
- b) Explain PLL with the help of neat block diagram (8)

Module 4

- 17 Using Quine McCluskey method simplify $f = \sum m(0,1,6,7,8,9,13,14,15)$ (14)
- 18 a) Design a 3 bit binary to gray code converter. (10)
- b) Design a half adder circuit using logic gates. (4)

Module 5

- 19 Design a 3-bit synchronous UP counter using JK flip-flop. (14)
- 20 Design a mod 6 asynchronous counter. (14)
