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Pages: 2

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (R, S) / S1 (PT) (S, FE) Examination December 2023 (2019 Scheme)

Course Code: EET205

Course Name: ANALOG ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1	List the factors to be considered while selecting the operating point of a transistor in an amplifier circuit.	(3)
2	What is the role of emitter bypass capacitor and coupling capacitors in an amplifier circuit?	(3)
3	Sketch the transfer characteristics of an n channel JFET given I_{DSS} = 15mA and V_p = -6V.	(3)
4	Define transconductance of JFET.	(3)
5	State and explain Bark-hausen's criteria for sustained oscillations.	(3)
6	A feedback amplifier has a voltage gain of 300 without feedback. Determine the voltage gain with feedback if feedback ratio is 0.2.	(3)
7	Write any six characteristics of an ideal operational amplifier.	(3)
8	Design a non-inverting amplifier for a gain of 12.	(3)
9	Derive the output voltage equation of an ideal differentiator with circuit diagram.	(3)
10	Explain zero crossing detector circuit with diagram and waveforms.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 (a)	Design a voltage divider bias circuit for an operating point of I_C = 2mA and V_{CE} = 8V. Given V_{CC} = 20V, β = 100, V_{BE} = 0.7V, V_E =2V.	(10)
(b)	Define stability factor. Derive an expression for stability factor.	(4)
12 (a)	Draw the small signal ac equivalent circuit of common emitter amplifier using h parameters. Also derive the expressions for voltage gain, current gain, input impedance and output impedance.	(10)
(b)	How bias compensation is done using diodes?	(4)

Module 2

13 (a) Explain, with neat diagram, the construction and working of n-channel enhancement mode MOSFET. (10)

(b) Explain the hybrid pi model of BJT. (4)

14 (a) Draw the frequency response of common emitter amplifier. State the reasons for reduction of gain at low frequencies and high frequencies. (7)

(b) Using small signal equivalent circuit, derive the expression for voltage gain of common drain JFET amplifier. (7)

Module 3

15 (a) Define conversion efficiency of power amplifier. Derive the maximum conversion efficiency of transformer coupled class A power amplifier. (7)

(b) Design a RC phase shift oscillator circuit for a frequency of 2 kHz. (7)

16 (a) Derive the expression for frequency of oscillation of Wein bridge oscillator circuit with neat diagram. (10)

(b) Mention the merits and demerits of transformer coupled amplifier. (4)

Module 4

17 (a) Determine the output voltage of an op-amp for input voltages of $V_1 = 120$ mV and $V_2 = 110$ mV. The amplifier has a differential gain of $A_d = 4000$ and the value of CMRR is 100. (7)

(b) Explain the concept of virtual ground. What is the limiting value of output voltage of an op-amp. Justify your answer. (7)

18 (a) Design a summing amplifier that satisfies the output equation $V_0 = -(V_1 + 5V_2 + 2V_3)$. (7)

(b) Explain instrumentation amplifier with diagram. (7)

Module 5

19 (a) Explain the working of Schmitt trigger circuit with diagram and waveforms. (7)

(b) Explain the working of triangular wave generator using op-amp with diagram and waveforms. (7)

20 (a) Draw and explain the internal diagram of 555 timer IC. (7)

(b) Design an astable multivibrator using 555 timer for an output wave of 60% duty cycle at a frequency of 2 kHz. (7)