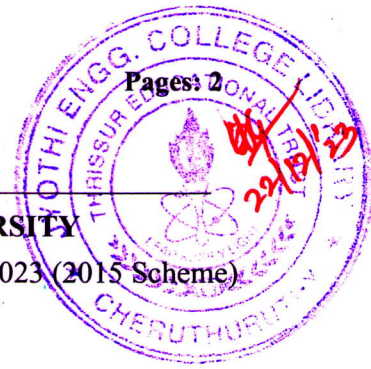E   08000CS207122301

Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
B.Tech Degree S3 (S, FE) / S1 (PT) (S, FE) Examination December 2023 (2015 Scheme)

Course Code: CS207

Course Name: Electronic Devices & Circuits

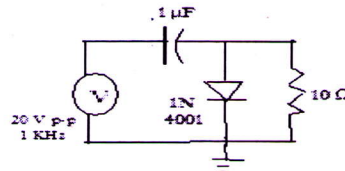Max. Marks: 100   Duration: 3 Hours

PART A
Answer all questions, each carries 3 marks.   Marks

1	Draw a differentiator circuit and draw the input and output waveforms for Square wave input.	(3)
2	Verify whether the following circuit will work as a clamper	(3)

3	Draw and explain the circuit of a 78XX IC based voltage regulator.	(3)
4	Draw and explain output characteristics of FET	(3)

PART B
Answer any two full questions, each carries 9 marks.

5	a)	Compare series and shunt voltage regulators.	(3)
	b)	Draw the characteristics and explain the working of an n-channel JFET.	(6)
6	a)	Draw and explain the circuit of a slicer for levels of -3V and -6V.	(4)
	b)	Draw and explain the block diagram of SMPS.	(5)
7	a)	Draw the circuit of a transistor shunt regulator and explain its working.	(5)
	b)	Assuming suitable values, design an integrator circuit for a 1 KHz square wave. Draw the relevant waveforms and circuit with designed components.	(4)

PART C
Answer all questions, each carries 3 marks.

8	Compare positive feedback with negative feedback.	(3)
9	Explain the effect of cascading on amplifier's gain and bandwidth.	(3)
10	What is mean by operating point of a transistor?	(3)
11	Draw the circuit diagram for bistable multivibrator and give a simple explanation?	(3)

PART D

Answer any two full questions, each carries 9 marks.

12 a) Draw the circuit diagram and explain the working of a common source MOSFET amplifier.   (4)

b) Draw the circuit diagram and explain the working of Wien bridge oscillator for an output frequency of 6 KHz.   (5)

13 a) With neat diagram explain the working of Hartley oscillator using BJT.   (4)

b) Derive the expression for frequency of oscillation and loop gain of a Hartley oscillator using BJT   (5)

14 With circuit diagram and design equations explain the working of a monostable multivibrator   (9)

PART E

Answer any four full questions, each carries 10 marks.

15 a) Define: (1) Slew rate, (2) CMRR, (3) offset voltage (4) Offset current   (8)

b) What are their practical values for parameters of op-amp IC 741   (2)

16 a) Draw the circuit diagram and frequency response of a second order high pass Butterworth filter using OP-AMP and explain its working.   (5)

b) Design a first order Butterworth LPF using OP-AMP for a high cut of frequency of 1KHz and pass band gain is 2.Give the design steps and draw the frequency response. (Assume C=0.01μF)   (5)

17 Using 555 timer, Explain the operation of monostable multivibrator with necessary waveforms.   (10)

18 a) Draw the circuit diagram of a 3-input summing amplifier using Op-Amp and explain its working with supporting derivations.   (5)

b) Sketch the circuit of an integrator circuit using Op-Amp and prove that the integration happens on the input signal.   (5)

19 a) Explain the concept of Binary weighted resistor DAC. What are its drawbacks? In a 10 bit DAC, Reference voltage is given as 15v. Find analog output for digital input of 1011011001.   (10)

20 a) With functional block diagram, explain the working of 555 Timer IC.   (4)

b) Write design equations and pin out of 555 TIMER IC working as astable Multivibrator to generate a wave form of 1KHz.,with 50% duty cycle.   (6)

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