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	D	APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY	
	В.Т	ech Degree S3 (S, FE) / S1 (PT) (S, FE) Examination December 2023 (2015 Scheme) C. C.
		MURI	JTH
		Course Code: CS203	
		Course Name: SWITCHING THEORY AND LOGIC DESIGN	
Ma	ax. M	farks: 100 Duration: 3	Hour
		PART A Answer all questions, each carries3 marks.	Mark
1		Convert the following numbers from the given base to the bases indicated	Mark
•	a)	(161.68) ₁₀ into Hexadecimal	(1)
	b)	$(-85)_{10}$ into 2's complement	(1)
	c)		(1)
2	c)	(11001001101.1011011) ₂ into octal	(1)
2		Represent decimal number $(-67)_{10}$ in single precision floating point format.	(3)
3	- \	Show the K-map contents for the following Boolean functions:	(2)
		$F = (\bar{x} + \bar{y})(y+z)$	(3)
	b)	$F = \sum m (0,2,7) + d (4)$	
4		State and prove Demorgan's theorems using gates	(3)
		PART B Answer any two full questions, each carries9 marks.	
5		Simplify the Boolean function $F=\sum (1,3,5,8,9,11,13,14,15)$ using Quine-	(9)
		McCluskey method.	
6	a)	Perform the following operations:	(4)
		i) $(F47)_{16} + (A2B)_{16}$ ii) $(745)_8 + (342)_8$	
	b)	Perform subtraction of the following using r's complement and (r-1)'s complement	(5)
		methods: 1000100 ₂ -1010101 ₂	
7	a)	Simplify the given Boolean function using Karnaugh Map and obtain the minimum	(5)
		Sum of Products expression $F=\sum (1,5,7,9,10,11,13,15)$	
	b)	i)Using the Boolean theorems simplify the following expression	(4)
		$F=ABC+\bar{A}B+AB\bar{C}$	
	×	ii) Find the complement of the function $F=X\overline{Y}+\overline{X}Y$	

PART C

Answer all questions, each carries3 marks.

8 Implement $F=A\bar{B} + B(C+D)$ with NAND gates (3)

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9		Implement the Boolean function F=∑m (1,3,6,7) using 4:1 MUX	(3)
10		Explain race around condition in flip flops	(3)
11		Differentiate between edge and level triggering	(3)
		PART D	
12	a)	Answer any two full questions, each carries 9 marks. A digital circuit has four inputs and one output. The output is equal to 1	(4)
		i) when an even number of inputs are equal to 1 ii) none of the inputs are equal to 1	
		and iii) any one input is 1	
	b)	Design a 2-bit magnitude comparator	(5)
13	a)	Explain state table and state diagram with an example.	(4)
	b)	Convert T Flip-Flop to JK Flip-Flop	(3)
	c)	Draw the circuit of JK flip flop with NAND gates only	(2)
14	a)	Design a 4-bit Gray to Binary code converter	(5)
	b)	Differentiate between truth table and excitation table. Write the truth and excitation	(4)
		table of RS flipflop	
		PART E	
1.5		Answer any four full questions, each carries 10 marks.	
15	a)	Design a synchronous counter with the following repeated binary sequence 0,2,5,7	(7)
		using T flip flop	
	b)	Explain serial adder	(3)
16		Draw a flow chart and explain the addition and subtraction of two binary numbers	(10)
		in signed magnitude representation	
17	a)	Compare RAM and ROM.	(3)
	b)	What is meant by HDL? Write an HDL code for a full adder in any of the modelling	(7)
10		styles.	
18	a)	Draw and explain 4-bit ring counter with its timing sequence.	(7)
	b)	Compare synchronous and asynchronous counter	(3)
19	a)	Implement the following Boolean functions using a $3 \times 4 \times 2$ PLA.	(6)
		$F1=\sum m (3,5,6,7)$ $F2=\sum m (0,2,5,7)$	
	b)	Explain the different types of ROMs.	(4)
20	2	Draw the circuit diagram of a 4-bit bidirectional shift register with parallel load	(10)
		and explain its working	
