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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S7 (S, FE) / S5 (PT) (S, FE) Examination December 2023 (2015 Scheme)

Course Code: CS405

Course Name: Computer System Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks. Marks

1		Explain implicit and explicit parallelism in parallel programming.	(4)
2		A 200MHz processor was used to execute a program with 200000 floating point instructions with clock cycle count of 1. Determine the execution time and MIPS rate for these programs.	(4)
3		Write notes on levels of memory and its speed cost comparison	(4)
4		What are the different flow control policies for collision resolution?	(4)
5		Explain Goodman's write-once protocol with state transition diagram.	(4)
6		Differentiate between store and forward and wormhole routing.	(4)
7		What is meant by pipeline stalling?	(4)
8		Write short notes on internal data forwarding	(4)
9		What are the four context switching policies adopted by multithreaded architectures?	(4)
10		How you can achieve instruction pipelining?	(4)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	Explain about the types of shared memory multiprocessor	(6)
	b)	State Amdahl's law. Write an expression for the overall speed up	(3)
12	a)	Consider the execution of the following code segment consisting of seven statements. Use Bernstein's conditions to detect the maximum parallelism embedded in this code. Justify the portions that can be executed in parallel and the remaining portions that must be executed sequentially.	(5)

S1: A=B+C
S2: C=D+E
S3: F=G+E
S4: C=A+F
S5: M=G+C
S6: A=L+E
S7: A=E+A

b) Explain Flynn's classification of computer architecture (4)

13 a) Explain memory hierarchy. (3)

b) Consider the design of a 3-level memory hierarchy with following features. Aim is to achieve effective memory access time Teff=850 ns, Cache hit ratio h1=0.98, Main memory Hit ratio h2=0.99, Total cost is upper bounded by$15000. Calculate the unknown specifications based on the given conditions (6)

Memory level	Access time	Capacity	Cost/k byte
Cache	t1 = 25ns	s1 = 512 KB	c1 = $1.25
Main memory	t2 = unknown	s2 = 32 MB	c2 = $0.2
Disk array	t3 = 25ns	s3 = unknown	c3 = $0.0002

PART C

Answer any two full questions, each carries 9 marks.

14 a) Explain how routing is done in 8 x 8 omega network. (7)

b) What are the reasons for cache inconsistence (2)

15 a) Explain the types of directory-based protocols. (5)

b) Demonstrate how asynchronous pipelining can be implemented. (4)

16 a) Consider a 16-node hypercube network. Based on the E-cube routing algorithm, show how to route a message from node (0111) to node (1101). All intermediate nodes must be identified on the routing path. (5)

b) Show the relations of speed up, throughput and efficiency of a k-stage linear pipeline model (4)

PART D

Answer any two full questions, each carries 12 marks.

17 a) Explain the problems of asynchrony. (6)

b) What are the solutions for the problems of asynchrony (6)

18 a) Write short notes on types of parallelism (6)

b) Compare Carry Save addition & carry propagation addition circuits. (6)

19 a) Explain Types of branch prediction & handling methods. (6)

b) Explain the types of hazards. (6)

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